Tikrit university

Collage of Engineering Shirqat

Department of Electrical Engineering

Second Class

Electronic II

Chapter 8

Lec 8

FET Amplifiers

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1 Introduction

Field-effect transistor amplifiers provide an excellent voltage gain with the added feature of a high input impedance. They are also low-power-consumption configurations with good frequency range and minimal size and weight. JFETs, depletion MOSFETs, and MESFETs can be used to design amplifiers having similar voltage gains. The depletion MOSFET (MESFET) circuit, however, has a much higher input impedance than a similar JFET configuration.

2 JFET Small-Signal Model

The ac analysis of a JFET configuration requires that a small-signal ac model for the JFET be developed. A major component of the ac model will reflect the fact that an ac voltage applied to the input gate-to-source terminals will control the level of current from drain to source.

The gate-to-source voltage controls the drain-to-source (channel) current of a JFET.

A dc gate-to-source voltage controls the level of dc drain current through a relationship known as Shockley's equation: $ID = IDSS\ (1 - VGS/VP)^2$. The change in drain current that will result from a change in gate-to-source voltage can be determined using the transconductance factor g_m in the following manner:

$$\Delta I_D = g_m \Delta V_{GS} \qquad (1)$$

$$g_m = \frac{\Delta I_D}{\Delta V_{GS}} \qquad (2)$$

2.1 Graphical Determination of g_m

If we now examine the transfer characteristics of Fig. 1, we find that gm is actually the slope of the characteristics at the point of operation. That is,

$$g_m = m = \frac{\Delta y}{\Delta x} = \frac{\Delta I_D}{\Delta V_{GS}} \qquad (3)$$

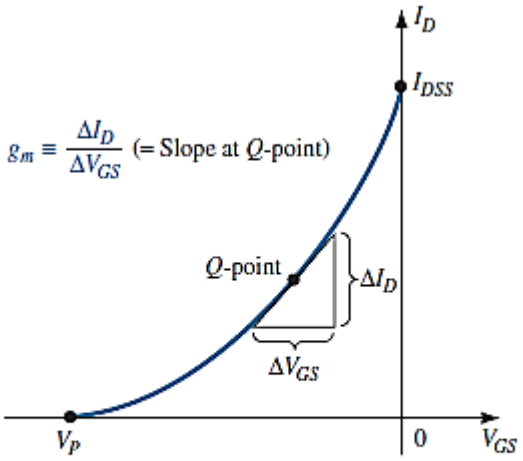

FIG. 1
Definition of g_m using transfer characteristic.

2.2 Mathematical Definition of g_m

The graphical procedure just described is limited by the accuracy of the transfer plot and the care with which the changes in each quantity can be determined.

The derivative of a function at a point is equal to the slope of the tangent line drawn at that point.

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{V_{GS}}{V_P}\right] \qquad (4)$$

where $|VP|$ denotes magnitude only, to ensure a positive value for *gm*. It was mentioned earlier that the slope of the transfer curve is a maximum at *VGS* = 0 V. Plugging in *VGS* = 0 V into Eq. (4) results in the following equation for the maximum value of *gm* for a JFET in which *IDSS* and *VP* have been specified

$$g_m = \frac{2I_{DSS}}{|V_P|}\left[1 - \frac{0}{V_P}\right]$$

$$g_{m0} = \frac{2I_{DSS}}{|V_P|} \qquad (5)$$

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] \qquad (6)$$

EXAMPLE 1 Determine the magnitude of g_m for a JFET with $I_{DSS} = 8\,\text{mA}$ and $V_P = -4\,\text{V}$ at the following dc bias points:

a. Find the maximum value of gm.

b. Find the value of gm at each operating point (1. VGs= -0.5, VGS= -1.5 and VGs=-2.5)

Solution:

a. $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(8\,\text{mA})}{4\,\text{V}} = \mathbf{4\,mS}$ (maximum possible value of g_m)

b. At $V_{GS} = -0.5\,\text{V}$,

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = 4\,\text{mS}\left[1 - \frac{-0.5\,\text{V}}{-4\,\text{V}}\right] = \mathbf{3.5\,mS}$$

At $V_{GS} = -1.5\,\text{V}$,

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = 4\,\text{mS}\left[1 - \frac{-1.5\,\text{V}}{-4\,\text{V}}\right] = \mathbf{2.5\,mS}$$

At $V_{GS} = -2.5\,\text{V}$,

$$g_m = g_{m0}\left[1 - \frac{V_{GS}}{V_P}\right] = 4\,\text{mS}\left[1 - \frac{-2.5\,\text{V}}{-4\,\text{V}}\right] = \mathbf{1.5\,mS}$$

On specification sheets, *gm* is often provided as *gfs* or *yfs*, where *y* indicates it is part of an admittance equivalent circuit. The *f* signifies *f*orward transfer conductance, and the *s* indicates that it is connected to the source terminal. In equation form,

$$g_m = g_{fs} = y_{fs} \qquad (7)$$

2.3 Effect of I_D on g_m

A mathematical relationship between gm and the dc bias current ID can be derived by noting that Shockley's equation can be written in the following form:

$$1 - \frac{V_{GS}}{V_P} = \sqrt{\frac{I_D}{I_{DSS}}} \qquad (8)$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS}}{V_P}\right) = g_{m0}\sqrt{\frac{I_D}{I_{DSS}}} \qquad (9)$$

the highest values of gm are obtained when VGS approaches 0 V and ID approaches its maximum value of IDSS.

2.4 JFET input impedance *Zi*

The input impedance of all commercially available JFETs is sufficiently large to assume that the input terminals approximate an open circuit. In equation form,

$$Z_i\,(\text{JFET}) = \infty\,\Omega \qquad (10)$$

For a JFET a practical value of 10^9 V (1000 MV) is typical, whereas a value of 10^{12} V to 10^{15} V is typical for MOSFETs and MESFETs.

2.5 JFET Output impedance *Zo*

The output impedance of JFETs is similar in magnitude to that of conventional BJTs. On JFET specification sheets, the output impedance will typically appear as *gos* or *yos* with the units of μS. The parameter *yos* is a component of an *admittance equivalent circuit*, with the subscript *o* signifying an *o*utput network parameter and *s* the terminal (source) to which it is attached in the model. For the JFET of Fig. 20, *gos* has a range of 10 μS to 50 μS or 20 kV ($R = 1/G = 1/50$ μS) to 100 kV ($R = 1/G = 1/10$ μS).

In equation form,

$$Z_o\,(\text{JFET}) = r_d = \frac{1}{g_{os}} = \frac{1}{y_{os}} \qquad (11)$$

The output impedance an often applied approximation. In equation form,

$$r_d = \left.\frac{\Delta V_{DS}}{\Delta I_D}\right|_{V_{GS}=\text{constant}} \qquad (12)$$

2.6 JFET Ac equivalent Circuit

Now that the important parameters of an ac equivalent circuit have been introduced and discussed, a model for the JFET transistor in the ac domain can be constructed. The control of *Id* by *Vgs* is included as a current source *gmVgs* connected from drain to source as shown in Fig. 8. The current source has its arrow pointing from drain to source to establish a 180° phase shift between output and input voltages as will occur in actual operation.

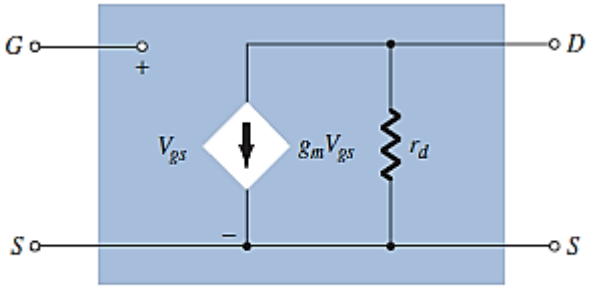

FIG. 8
JFET ac equivalent circuit.

The input impedance is represented by the open circuit at the input terminals and the output impedance by the resistor *rd* from drain to source. Note that the gate-to-source voltage is now represented by *Vgs* (lowercase subscripts) to distinguish it from dc levels. In addition, note that the source is common to both input and output circuits, whereas the gate and drain terminals are only in "touch" through the controlled current source *gmVgs*

In situations where *rd* is ignored (assumed sufficiently large in relation to other elements of the network to be approximated by an open circuit), the equivalent circuit is simply a current source whose magnitude is controlled by the signal *Vgs* and parameter *gm*—clearly a voltage-controlled current source.

EXAMPLE 6 Given $g_{fs} = 3.8$ mS and $g_{os} = 20\ \mu$S, sketch the FET ac equivalent model.

Solution:

$$g_m = g_{fs} = 3.8\text{ mS} \qquad \text{and} \qquad r_d = \frac{1}{g_{os}} = \frac{1}{20\ \mu\text{S}} = 50\text{ k}\Omega$$

resulting in the ac equivalent model of Fig. 9.

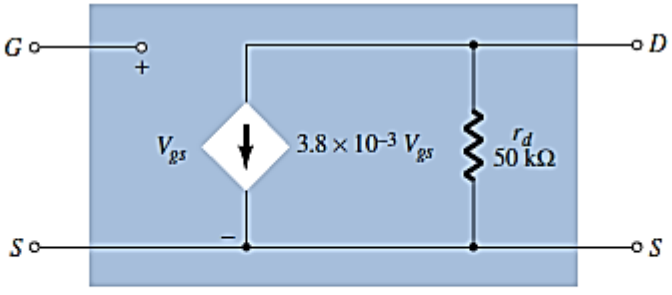

FIG. 9
JFET ac equivalent model for Example 6.

3 Fixed-Bias Configuration

Now that the JFET equivalent circuit has been defined, a number of fundamental JFET small-signal configurations are investigated. The approach parallels the ac analysis of BJT amplifiers with a determination of the important parameters of *Zi*, *Zo*, and *Av* for each configuration. The *fixed-bias* configuration of Fig. 10 includes the coupling capacitors *C*1 and *C*2, which isolate the dc biasing arrangement from the applied signal and load; they act as shortcircuit equivalents for the ac analysis.

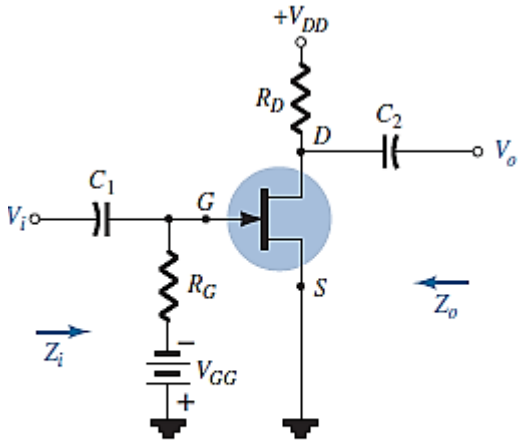

FIG. 10
JFET fixed-bias configuration.

Once the levels of gm and rd are determined from the dc biasing arrangement, specification sheet, or characteristics, the ac equivalent model can be substituted between the appropriate terminals as shown in Fig. 11. Note that both capacitors have the short-circuit equivalent because the reactance XC = 1/(2πfC) is sufficiently small compared to other impedance levels of the network, and the dc batteries VGG and VDD are set to 0 V by a short-circuit equivalent.

The network of Fig. 11 is then carefully redrawn as shown in Fig. 12. Note the defined polarity of Vgs, which defines the direction of gmVgs. If Vgs is negative, the direction of the current source reverses. The applied signal is represented by Vi and the output signal across $R_D \| rd$ by Vo.

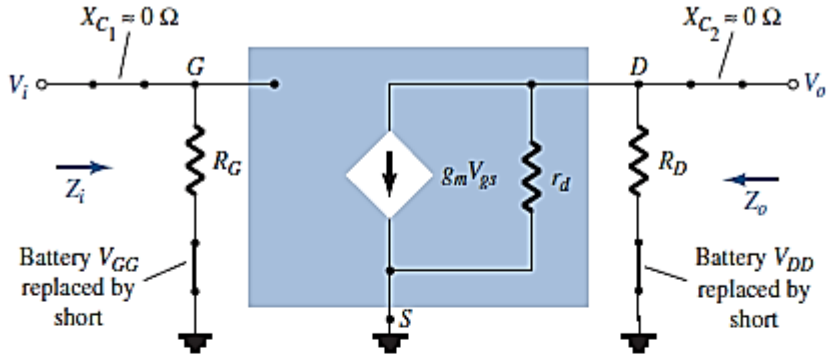

FIG. 11
Substituting the JFET ac equivalent circuit unit into the network of Fig. 10.

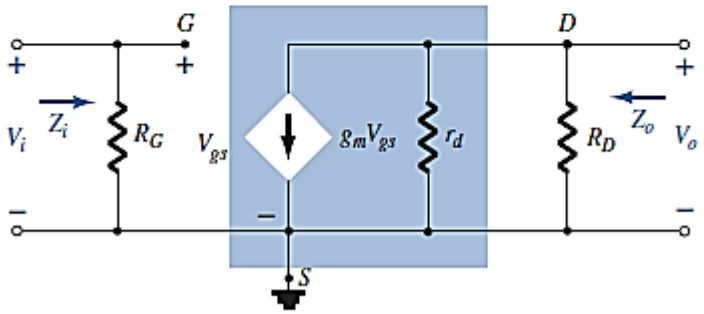

FIG. 12
Redrawn network of Fig. 11.

Zi Figure 12 clearly reveals that

$$Z_i = R_G \qquad (13)$$

because of the infinite input impedance at the input terminals of the JFET.

Zo Setting Vi = 0 V as required by the definition of Zo will establish Vgs as 0 V also. The result is gmVgs = 0 mA, and the current source can be replaced by an open-circuit equivalent as shown in Fig. 13. The output impedance is

$$Z_o = R_D \| r_d \qquad (14)$$

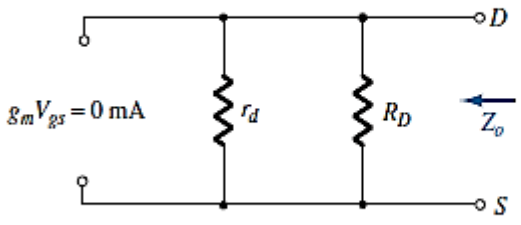

FIG. 13
Determining Z_o.

If the resistance rd is sufficiently large (at least 10:1) compared to RD, the approximation rd ‖RD ≈ RD can often be applied and

$$Z_o \cong R_D \qquad r_d \geq 10R_D \qquad (15)$$

A_v Solving for V_o in Fig. 12, we find

$$V_o = -g_m V_{gs}(r_d \| R_D)$$

but $$V_{gs} = V_i$$

and $$V_o = -g_m V_i(r_d \| R_D)$$

$$A_v = \frac{V_o}{V_i} = -g_m(r_d \| R_D) \qquad (16)$$

$$A_v = \frac{V_o}{V_i} = -g_m R_D \qquad r_d \geq 10R_D \qquad (17)$$

EXAMPLE 7 The fixed-bias configuration of Example 1 had an operating point defined by $V_{GS_Q} = -2$ V and $I_{D_Q} = 5.625$ mA, with $I_{DSS} = 10$ mA and $V_P = -8$ V. The network is redrawn as Fig. 14 with an applied signal V_i. The value of y_{os} is provided as 40 μS.

a. Determine g_m.
b. Find r_d.
c. Determine Z_i.
d. Calculate Z_o.
e. Determine the voltage gain A_v.
f. Determine A_v ignoring the effects of r_d.

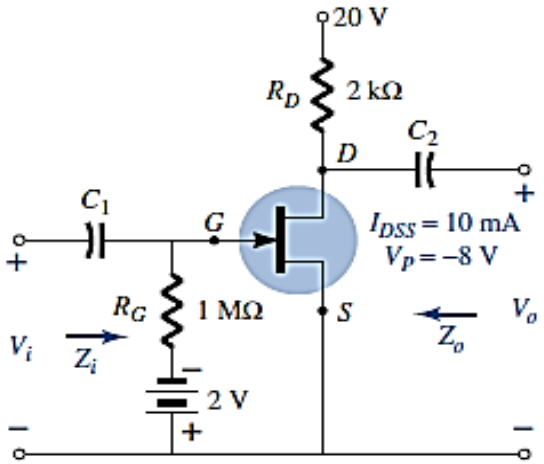

FIG. 14
JFET configuration for Example 7.

Solution:

a. $g_{m0} = \dfrac{2I_{DSS}}{|V_P|} = \dfrac{2(10\text{ mA})}{8\text{ V}} = 2.5\text{ mS}$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 2.5\text{ mS}\left(1 - \frac{(-2\text{ V})}{(-8\text{ V})}\right) = \mathbf{1.88\text{ mS}}$$

b. $r_d = \dfrac{1}{y_{os}} = \dfrac{1}{40\,\mu\text{S}} = \mathbf{25\,k\Omega}$

c. $Z_i = R_G = \mathbf{1\,M\Omega}$

d. $Z_o = R_D \| r_d = 2\,\text{k}\Omega \| 25\,\text{k}\Omega = \mathbf{1.85\,k\Omega}$

e. $A_v = -g_m(R_D \| r_d) = -(1.88\text{ mS})(1.85\,\text{k}\Omega)$

$= \mathbf{-3.48}$

f. $A_v = -g_m R_D = -(1.88\text{ mS})(2\,\text{k}\Omega) = \mathbf{-3.76}$

As demonstrated in part (f), a ratio of 25 kΩ:2 kΩ = 12.5:1 between r_d and R_D results in a difference of 8% in the solution.

4 Self-Bias Configuration

The fixed-bias configuration has the distinct disadvantage of requiring two dc voltage sources. The *self-bias* configuration of Fig. 15 requires only one dc supply to establish the desired operating point.

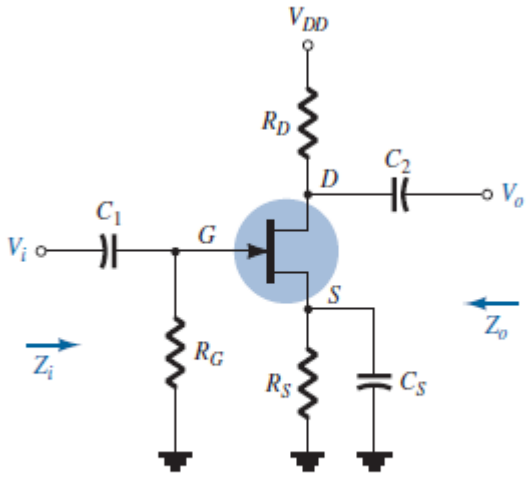

FIG. 15
Self-bias JFET configuration.

The capacitor *CS* across the source resistance assumes its open-circuit equivalence for dc, allowing *RS* to define the operating point. Under ac conditions, the capacitor assumes the short-circuit state and "short circuits" the effects of *RS*. If left in the ac, gain will be reduced, as will be shown in the paragraphs to follow.

The JFET equivalent circuit is established in Fig. 16 and carefully redrawn in Fig. 17. Since the resulting configuration is the same as appearing in Fig. 12, the resulting equations for *Zi*, *Zo*, and *Av* will be the same.

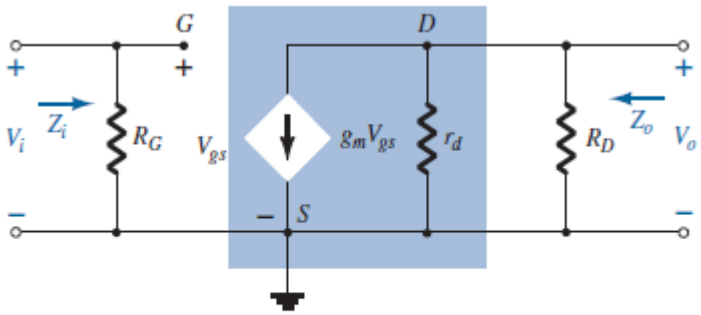

FIG. 17
Redrawn network of Fig. 16.

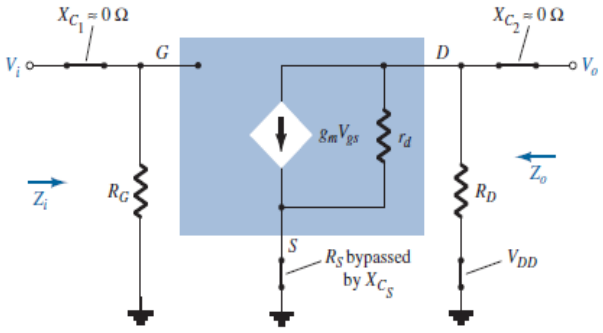

FIG. 16
Network of Fig. 15 following the substitution of the JFET ac equivalent circuit.

Z_i

$$Z_i = R_G \tag{18}$$

Z_o

$$Z_o = r_d \| R_D \tag{19}$$

If $r_d \geq 10R_D$,

$$Z_o \cong R_D \quad r_d \geq 10R_D \tag{20}$$

A_v

$$A_v = -g_m(r_d \| R_D) \tag{21}$$

If $r_d \geq 10R_D$,

$$A_v = -g_m R_D \quad r_d \geq 10R_D \tag{22}$$

phase relationship The negative sign in the solutions for *Av* again indicates a phase shift of 180° between *Vi* and *Vo*.

Unbypassed RS

If CS is removed from Fig 15, the resistor RS will be part of the ac equivalent circuit as shown in Fig. 18. In this case, there is no obvious way to reduce the network to lower its level of complexity. In determining the levels of Zi, Zo, and Av, one must be very careful with notation and defined polarities and direction. Initially, the resistance rd will be left out of the analysis to form a basis for comparison.

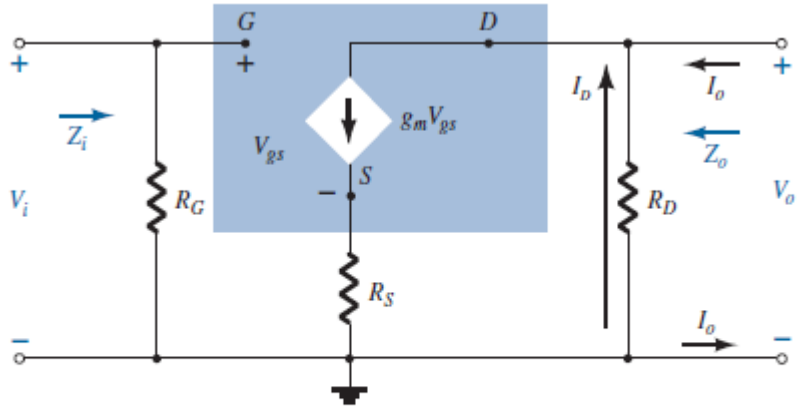

FIG. 18
Self-bias JFET configuration including the effects of R_S with $r_d = \infty\Omega$.

$$Z_i = R_G \tag{23}$$

$$Z_o = \frac{V_o}{I_o} = R_D \qquad r_d = \infty\Omega \tag{24}$$

$$Z_o \cong R_D \qquad r_d \geq 10R_D \tag{25b}$$

and

$$A_v = \frac{V_o}{V_i} = -\frac{g_m R_D}{1 + g_m R_S + \dfrac{R_D + R_S}{r_d}} \tag{26}$$

Again, if $r_d \geq 10(R_D + R_S)$,

$$A_v = \frac{V_o}{V_i} \cong -\frac{g_m R_D}{1 + g_m R_S} \qquad r_d \geq 10(R_D + R_S) \tag{27}$$

phase relationship The negative sign in Eq. (26) again reveals that a 180° phase shift will exist between Vi and Vo.

EXAMPLE 8 The self-bias configuration of Example 2 has an operating point defined by $V_{GS_Q} = -2.6$ V and $I_{D_Q} = 2.6$ mA, with $I_{DSS} = 8$ mA and $V_P = -6$ V. The network is redrawn as Fig. 20 with an applied signal V_i. The value of g_{os} is given as 20 μS.

a. Determine g_m.
b. Find r_d.
c. Find Z_i.
d. Calculate Z_o with and without the effects of r_d. Compare the results.
e. Calculate A_v with and without the effects of r_d. Compare the results.

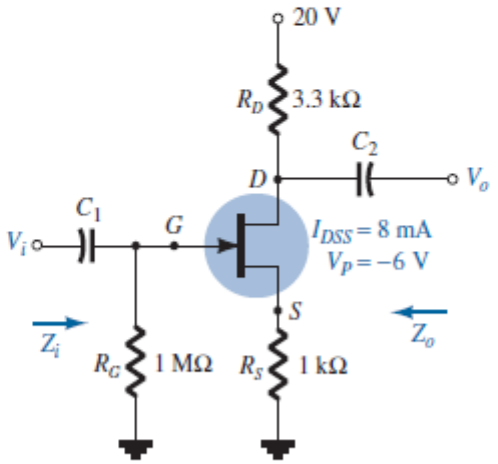

FIG. 20
Network for Example 8.

Solution:

a. $$g_{m0} = \frac{2I_{DSS}}{|V_P|} = \frac{2(8\text{ mA})}{6\text{ V}} = 2.67\text{ mS}$$

$$g_m = g_{m0}\left(1 - \frac{V_{GS_Q}}{V_P}\right) = 2.67\text{ mS}\left(1 - \frac{(-2.6\text{ V})}{(-6\text{ V})}\right) = \mathbf{1.51\text{ mS}}$$

b. $$r_d = \frac{1}{y_{os}} = \frac{1}{20\ \mu\text{S}} = \mathbf{50\ k\Omega}$$

c. $Z_i = R_G = \mathbf{1\ M\Omega}$

d. With r_d,

$$r_d = 50\text{ k}\Omega > 10R_D = 33\text{ k}\Omega$$

Therefore,

$$Z_o = R_D = \mathbf{3.3\ k\Omega}$$

If $r_d = \infty\,\Omega$,

$$Z_o = R_D = \mathbf{3.3\ k\Omega}$$

e. With r_d,

$$A_v = \frac{-g_m R_D}{1 + g_m R_S + \dfrac{R_D + R_S}{r_d}} = \frac{-(1.51\text{ mS})(3.3\text{ k}\Omega)}{1 + (1.51\text{ mS})(1\text{ k}\Omega) + \dfrac{3.3\text{ k}\Omega + 1\text{ k}\Omega}{50\text{ k}\Omega}}$$

$$= \mathbf{-1.92}$$

With $r_d = \infty\,\Omega$ (open-circuit equivalence),

$$A_v = \frac{-g_m R_D}{1 + g_m R_S} = \frac{-(1.51\text{ mS})(3.3\text{ k}\Omega)}{1 + (1.51\text{ mS})(1\text{ k}\Omega)} = \mathbf{-1.98}$$