Tikrit university

Collage of Engineering Shirqat

Department of Electrical Engineering

Second Class

Electronic II

Chapter 5
BJT AC Analysis

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1 Introduction

We now begin to examine the ac response of the BJT amplifier by reviewing the *models* most frequently used to represent the transistor in the sinusoidal ac domain.

One of our first concerns in the sinusoidal ac analysis of transistor networks is the magnitude of the input signal. It will determine whether *small-signal* or *large-signal* techniques should be applied. The small-signal technique is introduced in this chapter.

There are three models commonly used in the small-signal ac analysis of transistor networks: the r_e model, the hybrid π model, and the hybrid equivalent model.

2 Amplification in The Ac Domain

The transistor can be employed as an amplifying device. That is, the output sinusoidal signal (power) is greater than the input sinusoidal signal (power).

The question then arises as to how the ac power output can be greater than the input ac power. Conservation of energy dictates that over time the total power output, P_o, of a system cannot be greater than its power input, Pi, and that the efficiency defined by $\eta = P_o/P_i$ cannot be greater than 1. The factor missing from the discussion above that permits an ac power output greater than the input ac power is the applied dc power.

In fact, a *conversion efficiency* is defined by h = *Po*(ac)/*Pi*(dc), where *Po*(ac) is the ac power to the load and *Pi*(dc) is the dc power supplied.

Perhaps the role of the dc supply can best be described by first considering the simple dc network of Fig. 1. The resulting direction of flow is indicated in the figure with a plot of the current *i* versus time. Let us now insert a control mechanism such as that shown in Fig. 2. The control mechanism is such that the application of a relatively small signal to the control mechanism can result in a substantial oscillation in the output circuit.

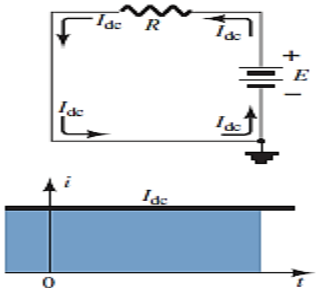

Fig. 1Steady current established by a dc supply .

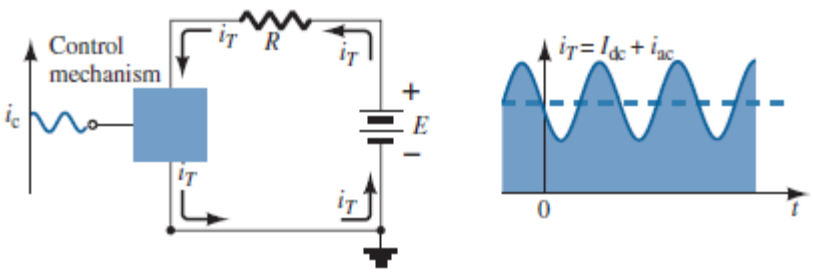

Fig. 2 Effect of a control element on the steady- state flow of the electrical system of Fig. 1.

For the system of Fig. 2, the peak value of the oscillation in the output circuit is controlled by the established dc level. Any attempt to exceed the limit set by the dc level will result in a "clipping" (flattening) of the peak region at the high and low end of the output signal.

The superposition theorem is applicable for the analysis and design of the dc and ac components of a BJT network, permitting the separation of the analysis of the dc and ac responses of the system.

3 BJT Transistor Modeling

A model is a combination of circuit elements, properly chosen, that best approximates the actual behaviour of a semiconductor device under specific operating conditions.

In an effort to demonstrate the effect that the ac equivalent circuit will have on the analysis to follow, consider the circuit of Fig. 3.

Because we are interested only in the ac response of the circuit, all the dc supplies can be replaced by a zero-potential equivalent (short circuit) because they determine only the dc (quiescent level) of the output voltage and not the magnitude of the swing of the ac output. This is clearly demonstrated by Fig. 4. The dc levels were simply important for determining the proper *Q*-point of operation. Once determined, the dc levels can be ignored in the ac analysis of the network. In addition, the coupling capacitors *C*1 and *C*2 and bypass capacitor *C*3 were chosen to have a very small reactance at the frequency of application. Therefore, they, too, may for all practical purposes be replaced by low resistance path or a short circuit.

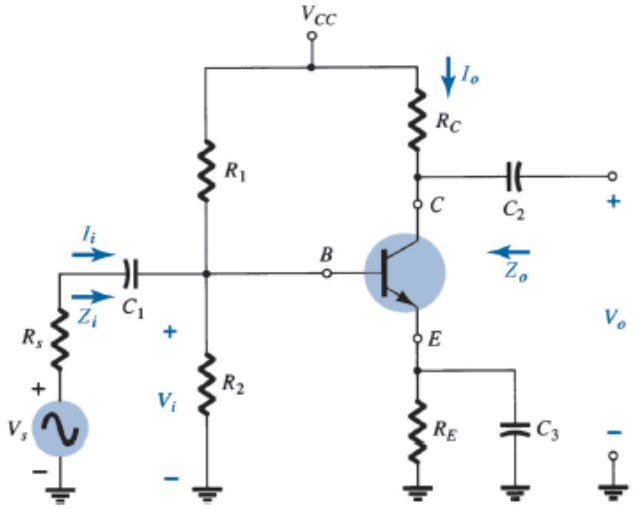

Fig. 3

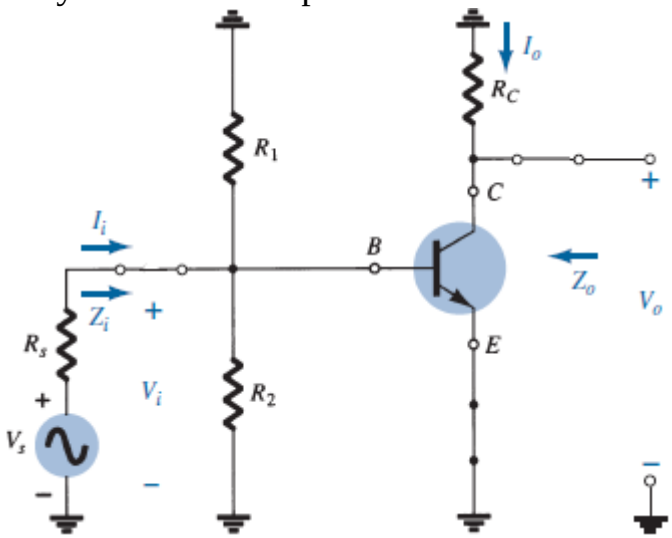

Fig. 4.

It is important as you progress through the modifications of the network to define the ac equivalent that the parameters of interest such as *Zi*, *Zo*, *Ii*, and *Io* as defined by Fig. 5 be carried through properly.

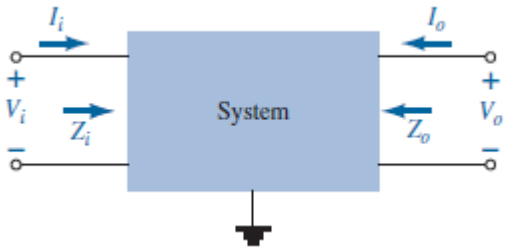

Fig. 5 Defining the important parameters.

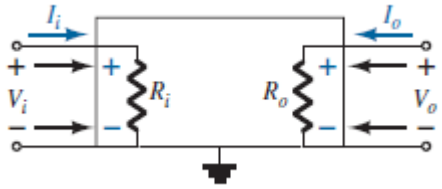

Fig. 6 ***Demonstrating the reason for the defined directions and polarities***

The parameters of Fig. 5 can be applied to any system whether it has one or a thousand components. In Fig. 5 the input current Ii and output current Io are, by definition, defined to enter the system. If, in a particular example, the output current is leaving the system rather than entering the system as shown in Fig. 5, a minus sign must be applied. The defined polarities for the input and output voltages are also as appearing in Fig. 5. If Vo has the opposite polarity, the minus sign must be applied. Note that Zi is the impedance "looking into" the system, whereas Zo is the impedance "looking back into" the system from the output side. Both the input impedance and output impedance are defined as having positive values.

For example, in Fig. 6 the input and output impedances for a particular system are both resistive. For the direction of *Ii* and *Io* the resulting voltage across the resistive elements will have the same polarity as *Vi* and *Vo*, respectively. If *Io* had been defined as the opposite direction in Fig. 5 a minus sign would have to be applied. For each case $Zi = Vi/Ii$ and $Zo = Vo/Io$ with positive results if they all have the defined directions and polarity of Fig. 5.

If we establish a common ground and rearrange the elements of Fig. 4, R1 and R2 will be in parallel, and RC will appear from collector to emitter as shown in Fig. 7. Because the components of the transistor equivalent circuit appearing in Fig. 7 employ familiar components such as resistors and independent controlled sources, analysis techniques such as superposition, Thévenin's theorem, and so on, can be applied to determine the desired quantities.

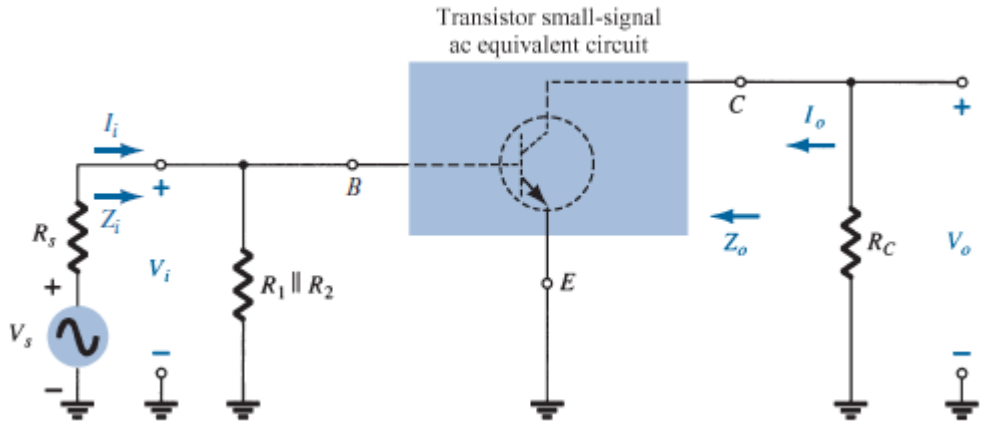

Fig. 7 Circuit of Fig. 4 redrawn for small-signal ac analysis.

Because we know that the transistor is an amplifying device, we would expect some indication of how the output voltage *Vo* is related to the input voltage *Vi*— the *voltage gain.* Note in Fig. 7 for this configuration that the *current gain* is defined by *Ai* = *Io*/*Ii*.

In summary, therefore, the ac equivalent of a transistor network is obtained by:

1. Setting all dc sources to zero and replacing them by a short-circuit equivalent

2. Replacing all capacitors by a short-circuit equivalent

3. Removing all elements bypassed by the short-circuit equivalents introduced by steps 1 and 2

4. Redrawing the network in a more convenient and logical form

4 The r_e Transistor Model

The re model for the CE, CB, and CC BJT transistor configurations will now be introduced with a short description of why each is a good approximation to the actual behaviour of a BJT transistor.

4.1 Common-emitter Configuration

The equivalent circuit for the common-emitter configuration will be constructed using the device characteristics and a number of approximations. Starting with the input side, we find the applied voltage *Vi* is equal to the voltage *Vbe* with the input current being the base current *Ib* as shown in Fig. 8.

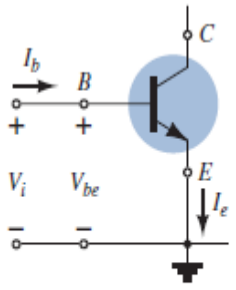

FIG. 8
Finding the input equivalent circuit for a BJT transistor.

For the equivalent circuit, therefore, the input side is simply a single diode with a current *Ie*, as shown in Fig. 10. However, we must now add a component to the network that will establish the current *Ie* of Fig. 10 using the output characteristics.

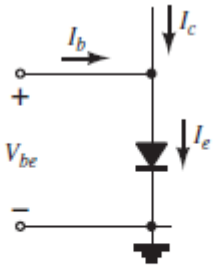

FIG. 10
Equivalent circuit for the input side

Because all the input and output parameters of the original configuration are now present, the equivalent network for the common-emitter configuration has been established in Fig. 12.

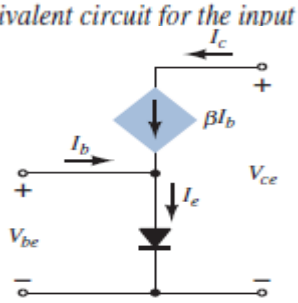

FIG. 12
BJT equivalent circuit.

It can be improved by first replacing the diode by its equivalent resistance as determined by the level of IE, as shown in Fig. 13. The diode resistance is determined by $r_D = 26\ mV/I_D$. Using the subscript e because the determining current is the emitter current will result in re = 26 mV/IE.

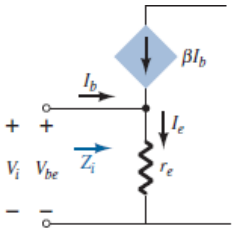

FIG. 13
Defining the level of Z_i.

Now, for the input side: $$Z_i = \frac{V_i}{I_b} = \frac{V_{be}}{I_b}$$

Solving for V_{be}: $$V_{be} = I_e r_e = (I_c + I_b) r_e = (\beta I_b + I_b) r_e$$
$$= (\beta + 1) I_b r_e$$

and $$Z_i = \frac{V_{be}}{I_b} = \frac{(\beta + 1) I_b r_e}{I_b}$$

$$\boxed{Z_i = (\beta + 1) r_e \cong \beta r_e} \qquad (1)$$

The result is that the impedance seen "looking into" the base of the network is a resistor equal to beta times the value of *re*, as shown in Fig. 14. The collector output current is still linked to the input current by beta as shown in the same figure.

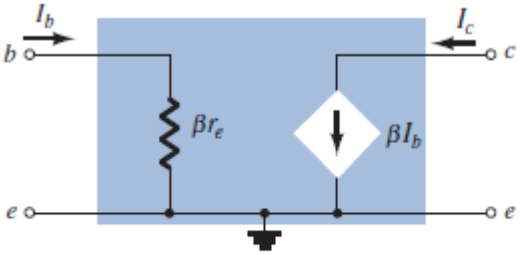

FIG. 14
Improved BJT equivalent circuit.

$$\boxed{r_o = \frac{\Delta V}{\Delta I} = \frac{V_A + V_{CE_Q}}{I_{C_Q}}} \qquad (2)$$

Typically, however, the Early voltage (V_A) is sufficiently large compared with the applied collector-to-emitter voltage to permit the following approximation.

$$r_o \cong \frac{V_A}{I_{C_Q}} \qquad (3)$$

Clearly, since V_A is a fixed voltage, the larger the collector current, the less the output impedance. For situations where the Early voltage is not available the output impedance can be found from the characteristics at any base or collector current using the following equation:

$$r_o = \frac{\Delta V_{CE}}{\Delta I_C} \qquad (4)$$

In any event, an output impedance can now be defined that will appear as a resistor in parallel with the output as shown in the equivalent circuit of Fig. 16.

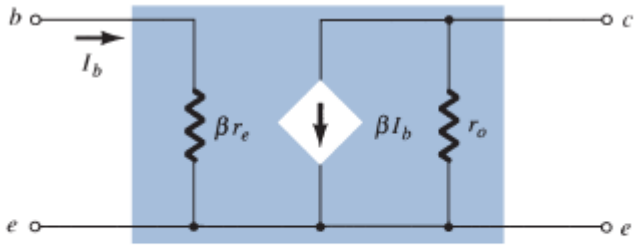

FIG. 16
r_e model for the common-emitter transistor configuration including effects of r_o.

The equivalent circuit of Fig. 16 will be used throughout the analysis to follow for the common-emitter configuration. Typical values of beta run from 50 to 200, with values of βr_e typically running from a few hundred ohms to a maximum of 6 kΩ to 7 kΩ. The output resistance r_o is typically in the range of 40 kΩ to 50 kΩ.

4.2 Common-base Configuration

The common-base equivalent circuit will be developed in much the same manner as applied to the common-emitter configuration. For the common-base configuration of Fig. 17a the *npn* transistor employed will present the same possibility at the input circuit.

The result is the use of a diode in the equivalent circuit as shown in Fig. 17b. For the output circuit, the collector current is related to the emitter current by alpha α. In this case, however, the controlled source defining the collector current as inserted in Fig. 17b is

opposite in direction to that of the controlled source of the common-emitter configuration. The direction of the collector current in the output circuit is now opposite that of the defined output current.

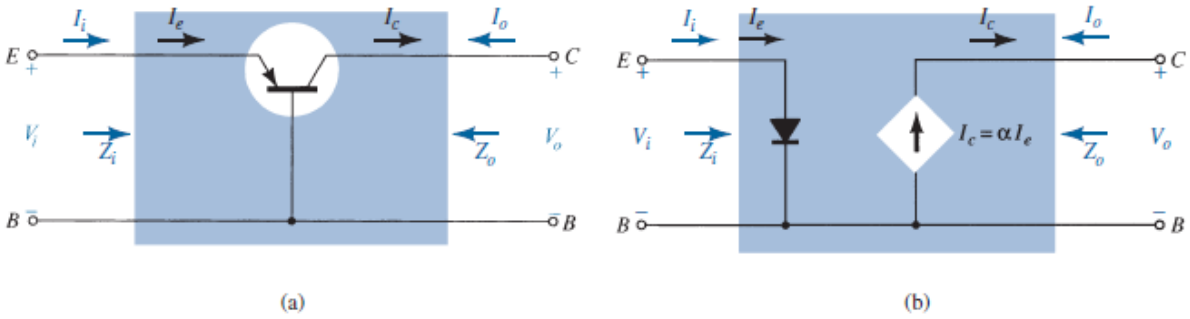

FIG. 17
(a) Common-base BJT transistor; (b) equivalent circuit for configuration of (a).

For the ac response, the diode can be replaced by its equivalent ac resistance determined by $r_e = 26\ \text{mv}/I_E$ as shown in Fig. 18. Take note of the fact that the emitter current continues to determine the equivalent resistance.

The network of Fig. 18 is therefore an excellent equivalent circuit for the analysis of most common-base configurations. It is similar in many ways to that of the common-emitter configuration. In general, common-base configurations have very low input impedance because it is essentially simply *re*. Typical values extend from a few ohms to perhaps 50 Ω. The output impedance *ro* will typically extend into the megohm range. Because the output current is opposite to the defined *Io* direction, you will find in the analysis to follow that there is no phase shift between the input and output voltages. For the common-emitter configuration there is a 180° phase shift.

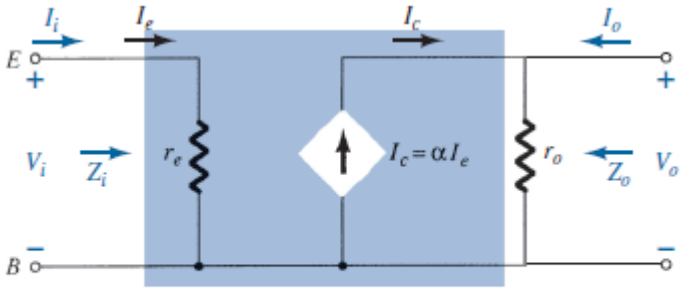

FIG. 18
Common base r_e equivalent circuit.

4.3 Common-Collector Configuration

For the common-collector configuration, the model defined for the common-emitter configuration of Fig. 16 is normally applied rather than defining a model for the common-collector configuration.

4.4 npn versus *pnp*

The dc analysis of *npn* and *pnp* configurations is quite different in the sense that the currents will have opposite directions and the voltages opposite polarities. However, for an ac analysis where the signal will progress between positive and negative values, the ac equivalent circuit will be the same.

5 Common-Emitter Fixed-Bias Configuration

The first configuration to be analyzed in detail is the common-emitter *fixed-bias* network of Fig. 20. Note that the input signal *Vi* is applied to the base of the transistor, whereas the output *Vo* is off the collector. In addition, recognize that the input current *Ii* is not the base current, but the source current, and the output current *Io* is the collector current. The small-signal ac analysis begins by removing the dc effects of *VCC* and replacing the dc blocking capacitors *C*1 and *C*2 by short-circuit equivalents, resulting in the network of Fig. 21.

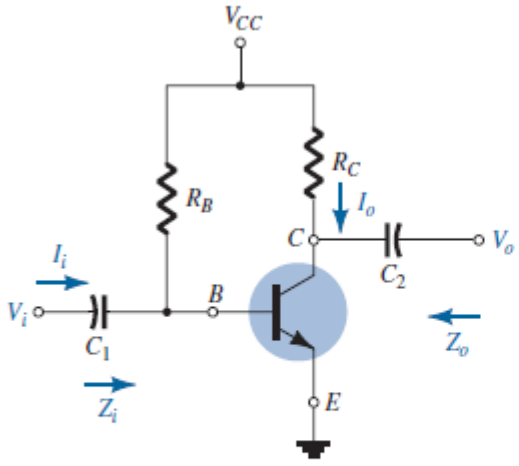

FIG. 20
Common-emitter fixed-bias configuration.

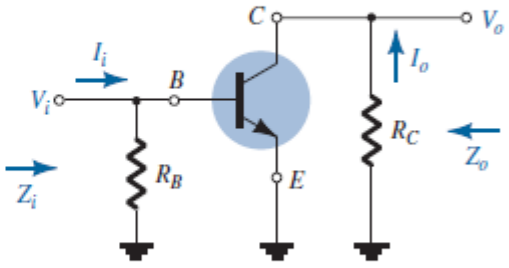

FIG. 21
Network of Fig. 20 following the removal of the effects of V_{CC}, C_1, and C_2.

Note in Fig. 21 that the common ground of the dc supply and the transistor emitter terminal permits the relocation of *RB* and *RC* in parallel with the input and output sections of the transistor, respectively. In addition, note the placement of the important network

parameters *Zi*, *Zo*, *Ii*, and *Io* on the redrawn network. Substituting the *re* model for the common-emitter configuration of Fig. 21 results in the network of Fig. 22.

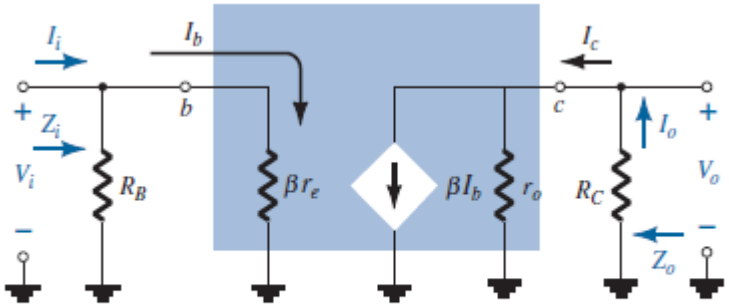

FIG. 22
Substituting the r_e model into the network of Fig. 21.

The value of *re* must be determined from a dc analysis of the system, and the magnitude of *ro* is typically obtained from the specification sheet or characteristics.

Zi Figure 22 clearly shows that

$$Z_i = R_B \| \beta r_e \quad \text{ohms} \qquad (5)$$

For the majority of situations RB is greater than bre by more than a factor of 10 (recall from the analysis of parallel elements that the total resistance of two parallel resistors is always less than the smallest and very close to the smallest if one is much larger than the other), permitting the following approximation:

$$Z_i \cong \beta r_e \quad \text{ohms} \qquad (6)$$
$$R_B \geq 10\beta r_e$$

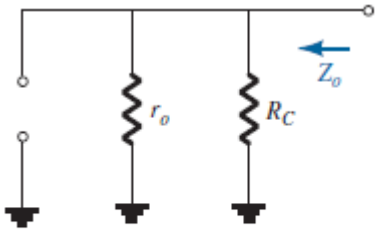

FIG. 23
Determining Z_o for the network of Fig. 22.

Zo Recall that the output impedance of any system is defined as the impedance *Zo* determined when *Vi* 5 0. For Fig. 22, when *Vi* = 0, *Ii* = *Ib* = 0, resulting in an open circuit equivalence for the current source. The result is the configuration of Fig. 23. We have

$$Z_o = R_C \| r_o \quad \text{ohms} \qquad (7)$$

If *ro* > 10RC, the approximation RC ‖ *ro* ≈ RC is frequently applied, and

$$Z_o \cong R_C \qquad (8)$$
$$r_o \geq 10R_C$$

AV The resistors ro and RC are in parallel, and

$$V_o = -\beta I_b (R_C \| r_o)$$

but $$I_b = \frac{V_i}{\beta r_e}$$

so that $$V_o = -\beta\left(\frac{V_i}{\beta r_e}\right)(R_C \| r_o)$$

and $$\boxed{A_v = \frac{V_o}{V_i} = -\frac{(R_C \| r_o)}{r_e}} \qquad (9)$$

If $ro \geq 10RC$, so that the effect of ro can be ignored,

$$\boxed{A_v = -\frac{R_C}{r_e}} \quad r_o \geq 10R_C \qquad (10)$$

Note the explicit absence of β in Eqs. (9) and (10), although we recognize that b must be utilized to determine re.

phase relationship The negative sign in the resulting equation for Av reveals that a 180° phase shift occurs between the input and output signals, as shown in Fig. 24. The is a result of the fact that βIb establishes a current through RC that will result in a voltage across RC, the opposite of that defined by Vo.

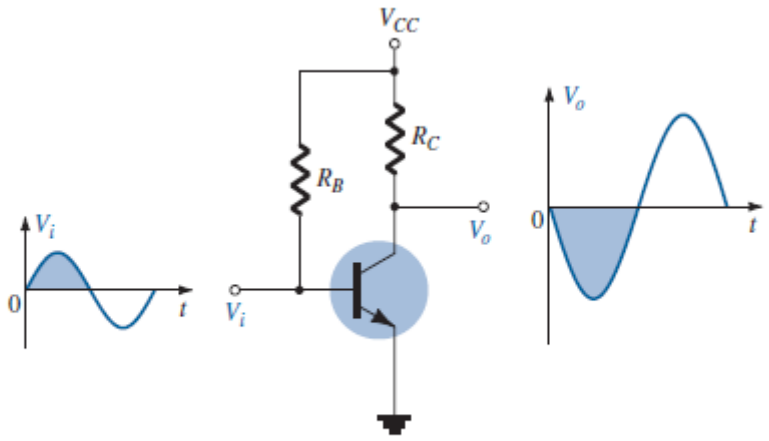

FIG. 24
Demonstrating the 180° phase shift between input and output waveforms.

EXAMPLE 1 For the network of Fig. 25:

a. Determine r_e.
b. Find Z_i (with $r_o = \infty\Omega$).
c. Calculate Z_o (with $r_o = \infty\Omega$).
d. Determine A_v (with $r_o = \infty\Omega$).
e. Repeat parts (c) and (d) including $r_o = 50\,\text{k}\Omega$ in all calculations and compare results.

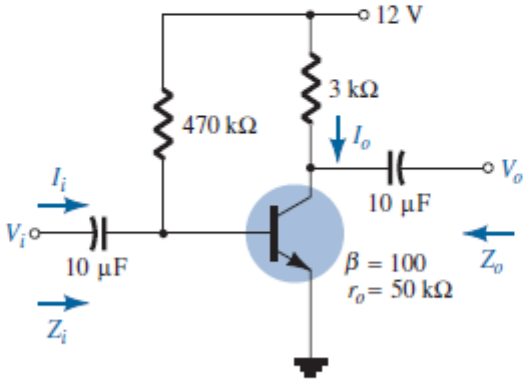

FIG. 25
Example 1.

Solution:

a. DC analysis:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\,\text{V} - 0.7\,\text{V}}{470\,\text{k}\Omega} = 24.04\,\mu\text{A}$$

$$I_E = (\beta + 1)I_B = (101)(24.04\,\mu\text{A}) = 2.428\,\text{mA}$$

$$r_e = \frac{26\,\text{mV}}{I_E} = \frac{26\,\text{mV}}{2.428\,\text{mA}} = \mathbf{10.71\ \Omega}$$

b. $\beta r_e = (100)(10.71\ \Omega) = 1.071\,\text{k}\Omega$

$$Z_i = R_B \| \beta r_e = 470\,\text{k}\Omega \| 1.071\,\text{k}\Omega = \mathbf{1.07\,k\Omega}$$

c. $Z_o = R_C = \mathbf{3\,k\Omega}$

d. $$A_v = -\frac{R_C}{r_e} = -\frac{3\,\text{k}\Omega}{10.71\ \Omega} = \mathbf{-280.11}$$

e. $Z_o = r_o \| R_C = 50\,\text{k}\Omega \| 3\,\text{k}\Omega = \mathbf{2.83\,k\Omega}$ vs. $3\,\text{k}\Omega$

$$A_v = -\frac{r_o \| R_C}{r_e} = \frac{2.83\,\text{k}\Omega}{10.71\ \Omega} = \mathbf{-264.24}\ \text{vs.}\ -280.11$$

6 Voltage-Divider Bias

The next configuration to be analyzed is the voltage-divider bias network of Fig. 26. Recall that the name of the configuration is a result of the voltage-divider bias at the input side to determine the dc level of VB.

Substituting the re equivalent circuit results in the network of Fig. 27. Note the absence of RE due to the low-impedance shorting effect of the bypass capacitor, CE. That is, at the frequency (or frequencies) of operation, the reactance of the capacitor is so small compared to RE that it is treated as a short circuit across RE. When VCC is set to zero, it places one end of R1 and RC at ground potential as shown in Fig. 27. In addition, note that R1 and R2 remain part of the input circuit, whereas RC is part of the output circuit. The parallel combination of R1 and R2 is defined by

$$R' = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2} \qquad (11)$$

Z_i From Fig. 27

$$Z_i = R' \| \beta r_e \qquad (12)$$

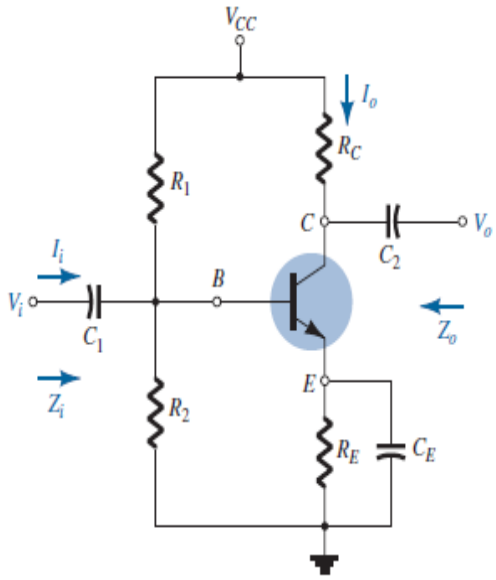

FIG. 26
Voltage-divider bias configuration.

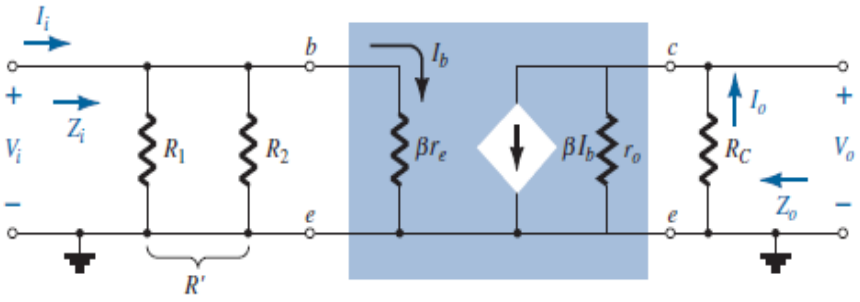

FIG. 27
Substituting the r_e equivalent circuit into the ac equivalent network of Fig. 26.

Z_o From Fig. 27 with V_i set to 0 V, resulting in $I_b = 0\ \mu A$ and $\beta I_b = 0$ mA,

$$\boxed{Z_o = R_C \| r_o} \tag{13}$$

If $r_o \geq 10R_C$,

$$\boxed{Z_o \cong R_C}_{r_o \geq 10R_C} \tag{14}$$

A_v Because R_C and r_o are in parallel,

$$V_o = -(\beta I_b)(R_C \| r_o)$$

and

$$I_b = \frac{V_i}{\beta r_e}$$

so that

$$V_o = -\beta\left(\frac{V_i}{\beta r_e}\right)(R_C \| r_o)$$

and

$$\boxed{A_v = \frac{V_o}{V_i} = \frac{-R_C \| r_o}{r_e}} \tag{15}$$

which you will note is an exact duplicate of the equation obtained for the fixed-bias configuration.

For $r_o \geq 10R_C$,

$$\boxed{A_v = \frac{V_o}{V_i} \cong -\frac{R_C}{r_e}}_{r_o \geq 10R_C} \tag{16}$$

phase relationship

The negative sign of Eq. (15) reveals a 180° phase shift between *Vo* and *Vi*.

Example 2 For the network of Fig. 28, determine:

a. re.

b. Zi.

c. Zo (ro = ∞).

d. Av (ro = ∞).

e. The parameters of parts (b) through (d) if ro = 50 kΩ and compare results.

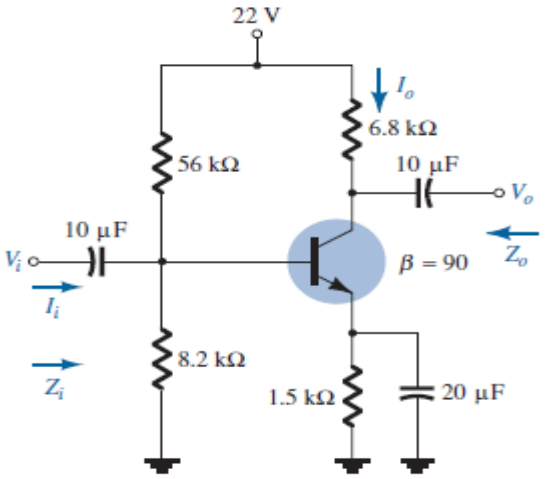

FIG. 28
Example 2.

Solution:

a. DC: Testing $\beta R_E > 10R_2$,

$$(90)(1.5\,\text{k}\Omega) > 10(8.2\,\text{k}\Omega)$$
$$135\,\text{k}\Omega > 82\,\text{k}\Omega \ (\textit{satisfied})$$

Using the approximate approach, we obtain

$$V_B = \frac{R_2}{R_1 + R_2}V_{CC} = \frac{(8.2\,\text{k}\Omega)(22\,\text{V})}{56\,\text{k}\Omega + 8.2\,\text{k}\Omega} = 2.81\,\text{V}$$
$$V_E = V_B - V_{BE} = 2.81\,\text{V} - 0.7\,\text{V} = 2.11\,\text{V}$$
$$I_E = \frac{V_E}{R_E} = \frac{2.11\,\text{V}}{1.5\,\text{k}\Omega} = 1.41\,\text{mA}$$
$$r_e = \frac{26\,\text{mV}}{I_E} = \frac{26\,\text{mV}}{1.41\,\text{mA}} = \mathbf{18.44\ \Omega}$$

b. $R' = R_1 \| R_2 = (56\,\text{k}\Omega) \| (8.2\,\text{k}\Omega) = 7.15\,\text{k}\Omega$

$Z_i = R' \| \beta r_e = 7.15\,\text{k}\Omega \| (90)(18.44\ \Omega) = 7.15\,\text{k}\Omega \| 1.66\,\text{k}\Omega$

$= \mathbf{1.35\,k\Omega}$

c. $Z_o = R_C = \mathbf{6.8\,k\Omega}$

d. $A_v = -\frac{R_C}{r_e} = -\frac{6.8\,\text{k}\Omega}{18.44\ \Omega} = \mathbf{-368.76}$

e. $Z_i = \mathbf{1.35\,k\Omega}$

$Z_o = R_C \| r_o = 6.8\,\text{k}\Omega \| 50\,\text{k}\Omega = \mathbf{5.98\,k\Omega}$ vs. $6.8\,\text{k}\Omega$

$A_v = -\frac{R_C \| r_o}{r_e} = -\frac{5.98\,\text{k}\Omega}{18.44\ \Omega} = \mathbf{-324.3}$ vs. -368.76

There was a measurable difference in the results for Z_o and A_v, because the condition $r_o \geq 10R_C$ was *not* satisfied.