Tikrit university

Collage of Engineering Shirqat

Department of Electrical Engineering

Second Class

Electronic II

Lec 10

Transistor Switching Networks

Prepared by

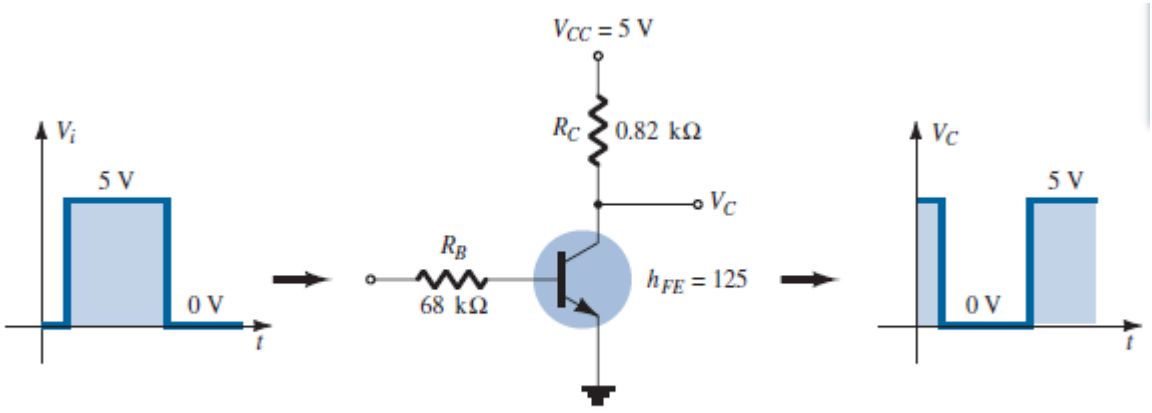
Asst Lecturer. Ahmed Saad Names

1. **BJT Switching Networks**

The application of transistors is not limited solely to the amplification of signals. Through proper design, transistors can be used as switches for computer and control applications. The network of Fig. 87a can be employed as an *inverter* in computer logic circuitry. Note that the output voltage *VC* is opposite to that applied to the base or input terminal. In addition, note the absence of a dc supply connected to the base circuit. The only dc source is connected to the collector or output side, and for computer applications is typically equal to the magnitude of the "high" side of the applied signal—in this case 5 V. The resistor *RB* will ensure that the full applied voltage of 5 V will not appear across the base-to-emitter junction. It will also set the *IB* level for the "on" condition.

Proper design for the inversion process requires that the operating point switch from cutoff to saturation along the load line depicted in Fig. 87b. For our purposes we will assume that $I_C = I_{CEO} \approx 0$ mA when $I_B = 0$ mA (an excellent approximation in light of improving construction techniques), as shown in Fig. 87b. In addition, we will assume that $V_{CE} = V_{CE\text{sat}} \approx 0$ V rather than the typical 0.1-V to 0.3-V level.

When *Vi* = 5 V, the transistor will be "on" and the design must ensure that the network is heavily saturated by a level of *IB* greater than that associated with the *IB* curve appearing



(a)

near the saturation level. In Fig. 87b, this requires that *IB* 7 50 mA. The saturation level for the collector current for the circuit of Fig. 87a is defined by

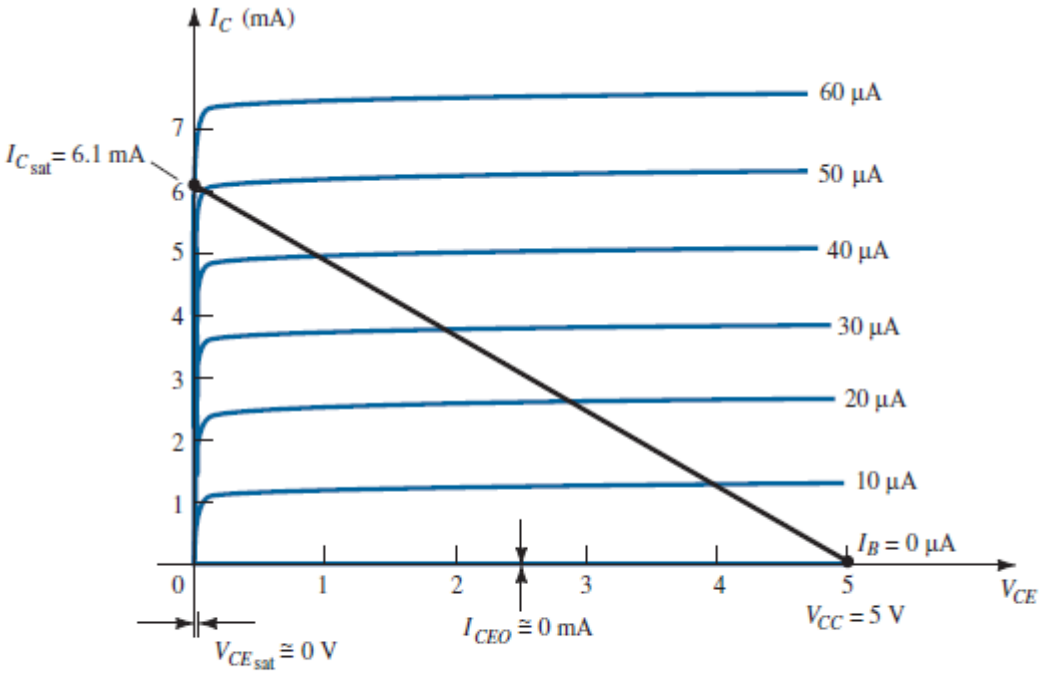
$$I_{C_{\text{sat}}} = \frac{V_{CC}}{R_C} \qquad (86)$$

The level of *IB* in the active region just before saturation results can be approximated by the following equation:

$$I_{B_{max}} \cong \frac{I_{C_{sat}}}{\beta_{dc}}$$

For the saturation level we must therefore ensure that the following condition is satisfied:

$$I_B > \frac{I_{C_{sat}}}{\beta_{dc}} \qquad (87)$$



(b)

FIG. 87
Transistor inverter.

For the network of Fig. 87b, when $V_i = 5$ V, the resulting level of I_B is

$$I_B = \frac{V_i - 0.7\text{ V}}{R_B} = \frac{5\text{ V} - 0.7\text{ V}}{68\text{ k}\Omega} = 63\ \mu\text{A}$$

and

$$I_{C_{sat}} = \frac{V_{CC}}{R_C} = \frac{5\text{ V}}{0.82\text{ k}\Omega} \cong 6.1\text{ mA}$$

Testing Eq. (87) gives

$$I_B = 63\ \mu\text{A} > \frac{I_{C_{sat}}}{\beta_{dc}} = \frac{6.1\text{ mA}}{125} = 48.8\ \mu\text{A}$$

which is satisfied. Certainly, any level of *IB* greater than 60 mA will pass through a *Q*-point on the load line that is very close to the vertical axis. For *Vi* = 0 V, *IB* = 0 mA, and because we are assuming that *IC* = *ICEO* = 0 mA, the voltage drop across *RC* as determined by *VRC* = *ICRC* = 0 V, resulting in *VC* = +5 V for the response indicated in Fig. 87a.

EXAMPLE 32 Determine R_B and R_C for the transistor inverter of Fig. 90 if $I_{C_{sat}} = 10$ mA.

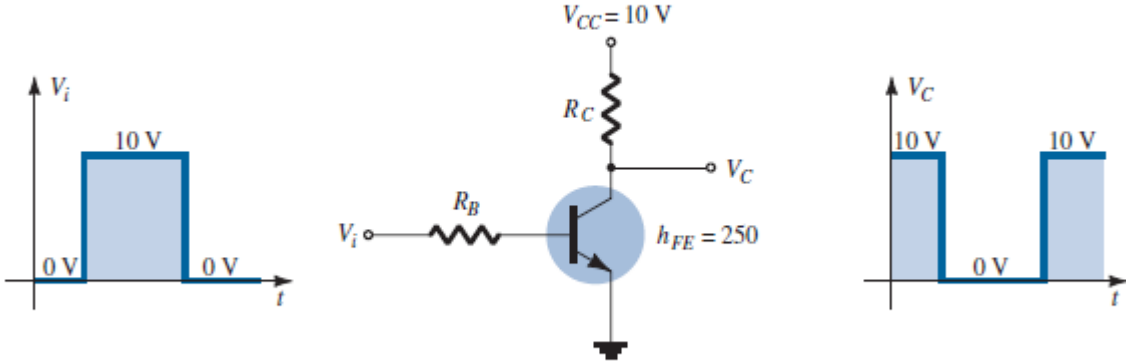


FIG. 90
Inverter for Example 32.

Solution: At saturation,

$$I_{C_{sat}} = \frac{V_{CC}}{R_C}$$

and

$$10\text{ mA} = \frac{10\text{ V}}{R_C}$$

so that

$$R_C = \frac{10\text{ V}}{10\text{ mA}} = 1\text{ k}\Omega$$

At saturation,

$$I_B \cong \frac{I_{C_{sat}}}{\beta_{dc}} = \frac{10\text{ mA}}{250} = 40\,\mu\text{A}$$

Choosing $I_B = 60\,\mu$A to ensure saturation and using

$$I_B = \frac{V_i - 0.7\text{ V}}{R_B}$$

we obtain

$$R_B = \frac{V_i - 0.7\text{ V}}{I_B} = \frac{10\text{ V} - 0.7\text{ V}}{60\,\mu\text{A}} = 155\text{ k}\Omega$$

Choose $R_B = 150\text{ k}\Omega$, which is a standard value. Then

$$I_B = \frac{V_i - 0.7\text{ V}}{R_B} = \frac{10\text{ V} - 0.7\text{ V}}{150\text{ k}\Omega} = 62\,\mu\text{A}$$

and

$$I_B = 62\,\mu\text{A} > \frac{I_{C_{sat}}}{\beta_{dc}} = 40\,\mu\text{A}$$

Therefore, use $R_B = \mathbf{150\text{ k}\Omega}$ and $R_C = \mathbf{1\text{ k}\Omega}$.

FET Switching Network

The MOSFET can be used as a switch in a wide variety of electronic applications. The transistor switch provides an advantage over mechanical switches in both speed and reliability. The transistor switch considered in this section is also called an inverter. Figure 2 shows the n-channel enhancement-mode MOSFET inverter circuit. If $vI < V_{GSTH}$, the transistor is in cutoff and iD = 0. There is no voltage drop across RD, and the output voltage is v_O = VDD. Also, since iD = 0, no power is dissipated in the transistor.

If $VI > V_{GSTH}$, the transistor is on and initially is biased in the saturation region, since VDS > VGS − V_{GSTH} . As the input voltage increases, the drain-to-source voltage decreases, and the transistor eventually becomes biased in the nonsaturation region.

When vI = VDD, the transistor is biased in the nonsaturation region, V_O reaches a minimum value

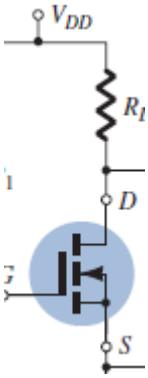


Fig 2