Digital System Design

Electrical Department-Fourth Stage

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Timing Circuits

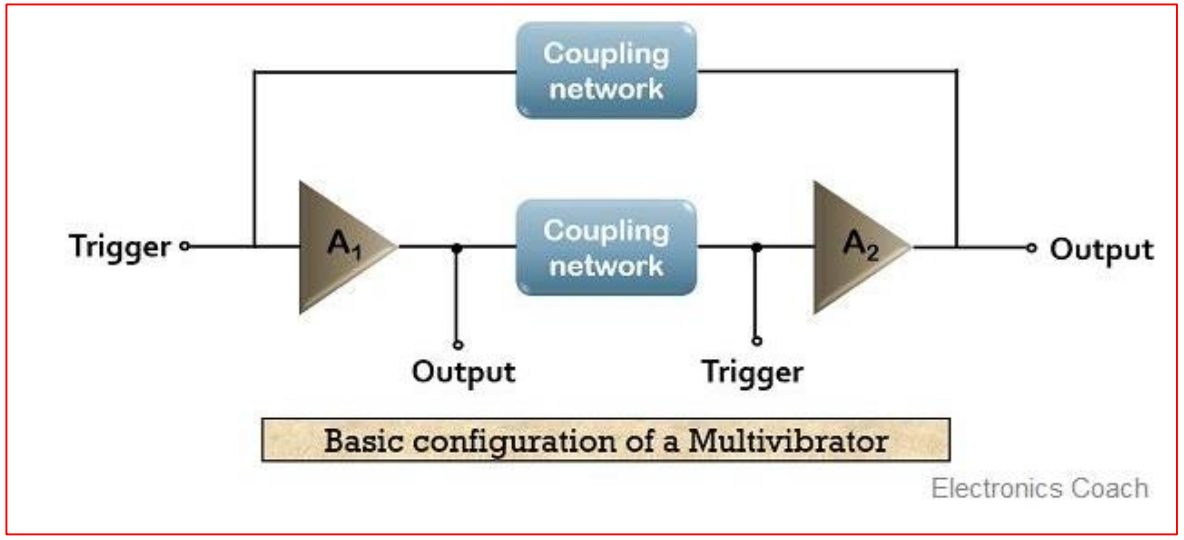
- **Bistable, Monostable and A stable Multiviberators**

Outlines

- What is a Multivibrator?
- What is a storge element?
- Bistable Multivibrator
- The S-R (SET-RESET) Latch
- The Gated S-R Latch
- The Gated D Latch
- Flip-Flops
- The D Flip-Flops
- The J-K Flip-Flop

What is a Multivibrator?

- An electronic device that produces a non-sinusoidal waveform as its output is known as a Multivibrator. The generated non-sinusoidal waveforms are basically a square wave, rectangular wave, a triangular wave, sawtooth wave, or ramp wave etc.
- It is a 2 stage RC coupled amplifier that operates in two modes. The modes are basically termed as states of the multivibrator.
- Two amplifiers are employed in which the output from the 1st stage acts as input to the 2nd stage. The output of the 2nd stage is then through a feedback path is provided to the input of the 1st stage.
- The operation of the circuit is controlled by two conditions on and off of the circuit. It performs oscillations between high and low state i.e., 0 and 1 thereby generating a continuous output.



Storage elements

- A storage element in a digital circuit can maintain a binary state indefinitely (as long as power is delivered to the circuit), until directed by an input signal to switch states.

- The major differences among various types of storage elements are in the number of inputs they possess and in the manner in which the inputs affect the binary state.

- Storage elements that operate with signal levels (rather than signal transitions) are referred to as latches; those controlled by a clock transition are flip-flops.

- Latches are said to be level-sensitive devices; flip-flops are edge-sensitive devices.

- The two types of storage elements are related because latches are the basic circuits from which all flip-flops are constructed.

- Although latches are useful for storing binary information and for the design of asynchronous sequential circuits, they are not practical for use as storage elements in synchronous sequential circuits.

- Because they are the building blocks of flip-flops, however, we will now consider the fundamental storage mechanism used in latches before considering flip-flops in the next sections.

Bistable Multivibrator

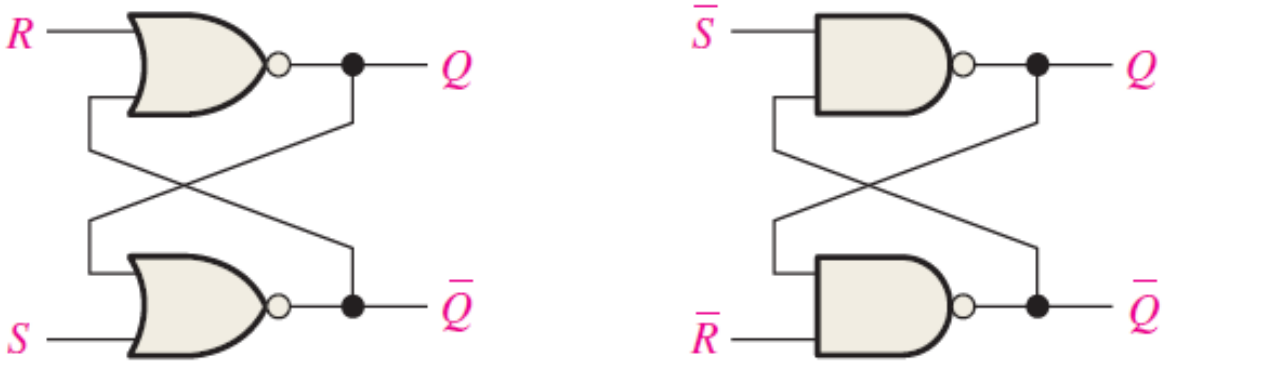
- A Bistable Multivibrator has two stable states. The circuit stays in any one of the two stable states. It continues in that state, unless an external trigger pulse is given.

- Two categories of bistable devices are the latch and the flip flop.

- Bistable devices have two stable states, called SET and RESET; they can retain either of these states indefinitely, making them useful as storage devices.

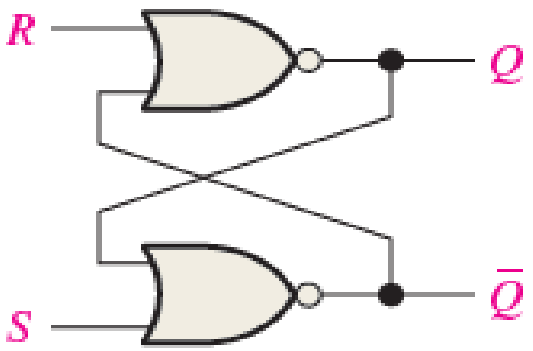
The S-R (SET-RESET) Latch

- A latch is a basic data storage element that can store one bit of data.
- A latch is a type of bistable logic device or multivibrator.
- An active-HIGH input S-R (SET-RESET) latch is formed with two cross-coupled NOR gates, as shown in Figure 1 (a).
- An active-LOW input $\overline{S}$-$\overline{R}$ latch is formed with two cross-coupled NAND gates, as shown in Figure 1 (b).



(a) Active-HIGH input S-R latch (b) Active-LOW input $\overline{S}$-$\overline{R}$ latch

- **An active-HIGH input S-R (SET-RESET) latch built with NOR gates**



(a) Active-HIGH input S-R latch

S	R	Q	$\bar{Q}$	Comment
0	0	NC	NC	**No Change, latch Remains in present state**
0	1	0	1	**RESET**
1	0	1	0	**SET**
1	1	0	0	**invalid**

- When both inputs, R and S, are equal to 0 the latch maintains its existing state because of the feedback loop. This state may be either Q = 0 and $\bar{Q}$ = 1, or Q = 1 and $\bar{Q}$ = 0, which is indicated in the table by stating that the Q and $\bar{Q}$ outputs have values 0/1 and 1/0, respectively.

- When R = 1 and S = 0, the latch is **reset** into a state where Q = 0 and $\bar{Q}$ = 1. When R = 0 and S = 1, the latch is **set** into a state where Q = 1 and $\bar{Q}$= 0.

- The fourth possibility is to have R = S = 1. In this case both Q and $\bar{Q}$ will be 0. The table in Table 1 resembles a truth table..

- **Notice that the output of each gate is connected to an input of the opposite gate. This produces the regenerative feedback that is characteristic of all latches and flip-flops.**

- **The NAND gate $\overline{S} - \overline{R}$ latch in Figure 1 (b). This latch is redrawn in Figure 2 with the negative-OR equivalent symbols used for the NAND gates. This is done because LOWs on the $\overline{S}$ and lines are the activating inputs. The latch in Figure 2 has two inputs, $\overline{S}$ and $\overline{R}$ and two outputs, Q and $\overline{Q}$. Let's start by assuming that both inputs and the Q output are HIGH, which is the normal latched state. Since the Q output is connected back to an input of gate G2, and the $\overline{R}$ input is HIGH, the output of G2 must be LOW. This LOW output is coupled back to an input of gate G1, ensuring that its output is HIGH. When the Q output is HIGH, the latch is in the SET state. It will remain in this state indefinitely until a LOW is temporarily applied to the $\overline{R}$ input. With a LOW on the $\overline{R}$ input and a HIGH on $\overline{S}$ the output of gate G2 is forced HIGH. This HIGH on the $\overline{Q}$ output is coupled back to an input of G1, and since the $\overline{S}$ input is HIGH, the output of G1 goes LOW. This LOW on the Q output is then coupled back to an input of G2, ensuring that the $\overline{Q}$ output remains HIGH even when the LOW on the $\overline{R}$ input is removed. When the Q output is LOW, the latch is in the RESET state. Now the latch remains indefinitely in the RESET state until a momentary LOW is applied to the $\overline{S}$ input.**

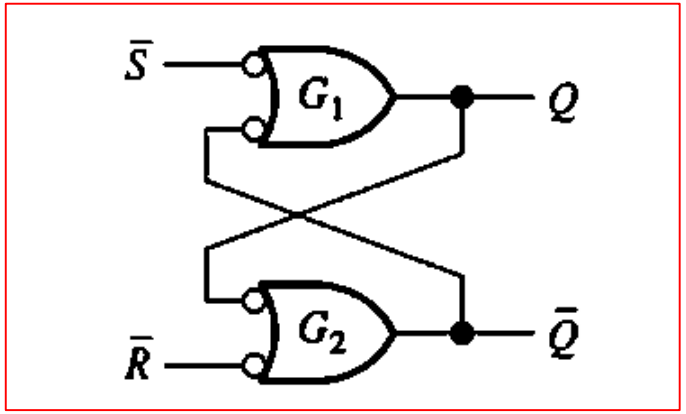


FIGURE 2 Negative-OR equivalent of the NAND gate $\overline{S} - \overline{R}$ latch in Figure 1(b).

- **In normal operation, the outputs of a latch are always complements of each other. When Q is HIGH, $\overline{Q}$ is LOW, and when Q is LOW, $\overline{Q}$ is HIGH.**

An invalid condition in the operation of an active-LOW input $\overline{S}$-$\overline{R}$ latch occurs when LOWs are applied to both $\overline{S}$ and $\overline{R}$ at the same time. As long as the LOW levels are simultaneously held on the inputs, both the Q and $\overline{Q}$ outputs are forced HIGH, thus violating the basic complementary operation of the outputs. Also, if the LOWs are released simultaneously, both outputs will attempt to go LOW. Since there is always some small difference in the propagation delay time of the gates, one of the gates will dominate in its transition to the LOW output state. This, in turn, forces the output of the slower gate to remain HIGH. In this situation, you cannot reliably predict the next state of the latch.

SET means that the Q output is HIGH.

Figure 7–3 illustrates the active-LOW input $\overline{S}$-$\overline{R}$ latch operation for each of the four possible combinations of levels on the inputs. (The first three combinations are valid, but the last is not.) Table 7–1 summarizes the logic operation in truth table form. Operation of the active-HIGH inpu NOR gate latch in Figure 7–1(a) is similar but requires the use of opposite logic levels.

RESET means that the Q output is LOW.

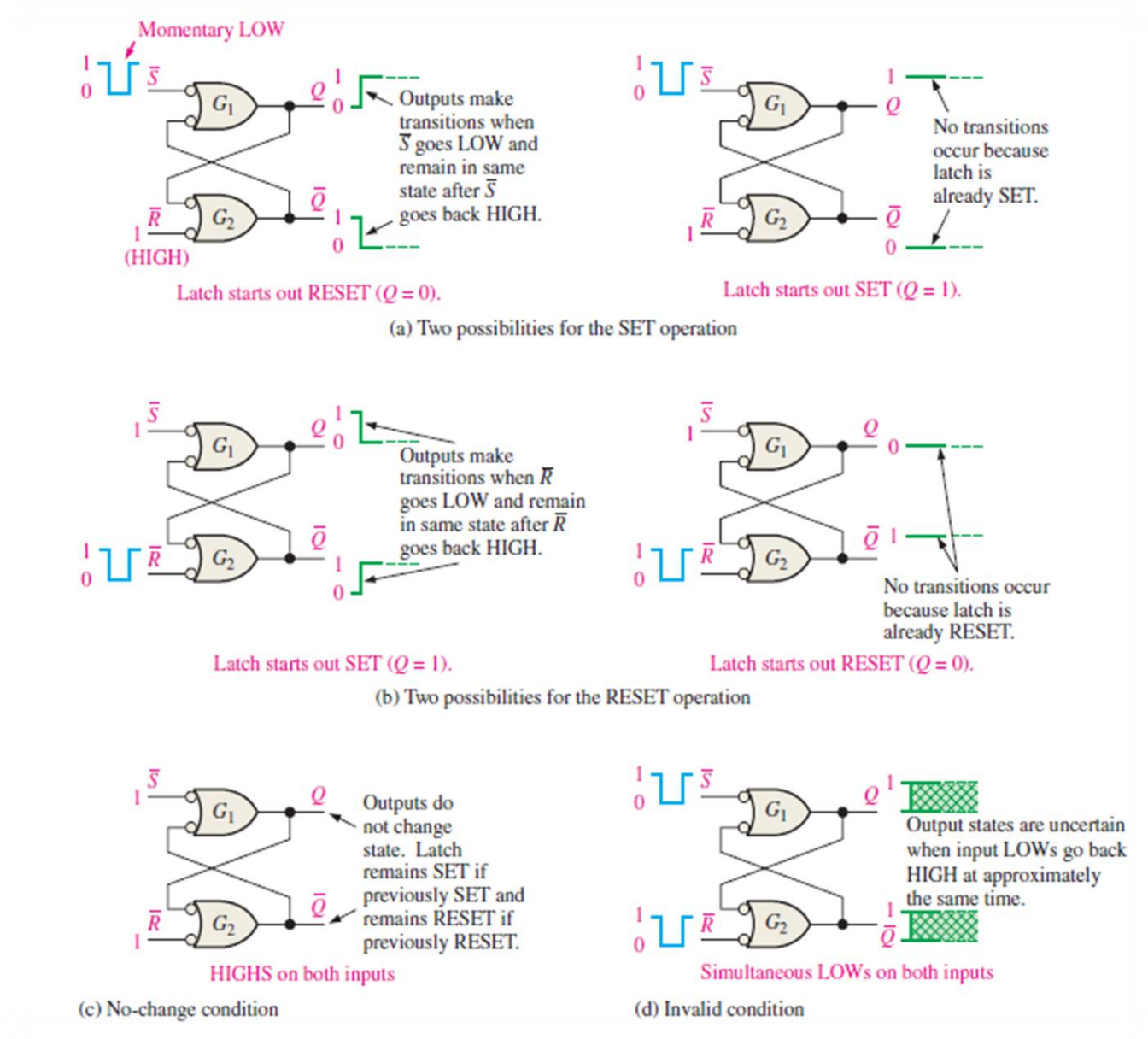


FIGURE 3 The three modes of basic $\overline{S}$-$\overline{R}$ latch operation (SET, RESET, no-change) and the invalid condition.

TABLE 1

Truth table for an active-LOW input $\overline{S}$-$\overline{R}$ latch.

Inputs		Outputs		
$\overline{S}$	$\overline{R}$	Q	$\overline{Q}$	Comments
1	1	NC	NC	No change. Latch remains in present state.
0	1	1	0	Latch SET.
1	0	0	1	Latch RESET.
0	0	1	1	Invalid condition

➢ **Logic symbols for both the active-HIGH input and the active-LOW input latches are shown in Figure 4.**

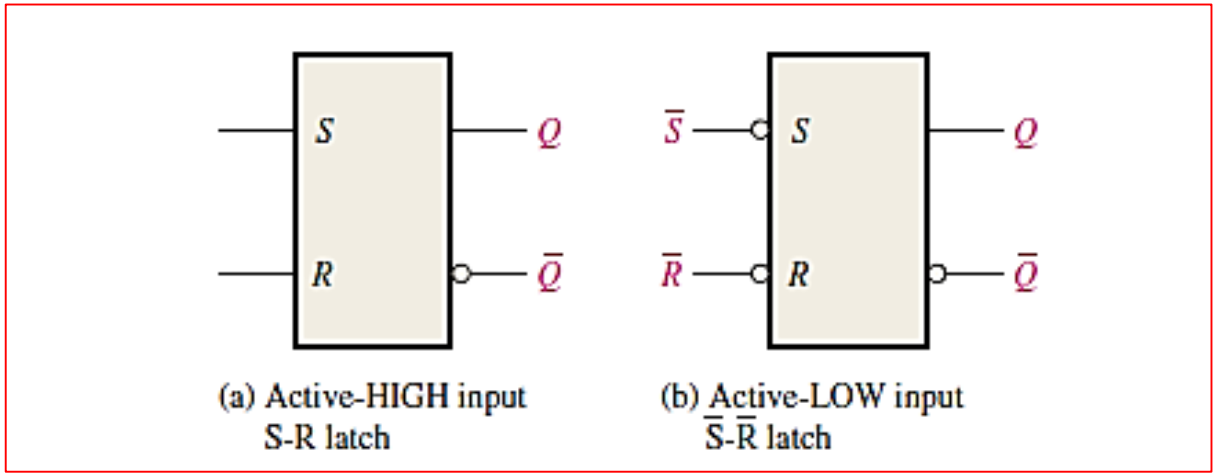


FIGURE 4 Logic symbols for the S-R and $\overline{S}$-$\overline{R}$ latch

EXAMPLE 1

If the $\overline{S}$ and $\overline{R}$ waveforms in Figure 5(a) are applied to the inputs of the latch in Figure 4(b), determine the waveform that will be observed on the Q output. Assume that Q is initially LOW.

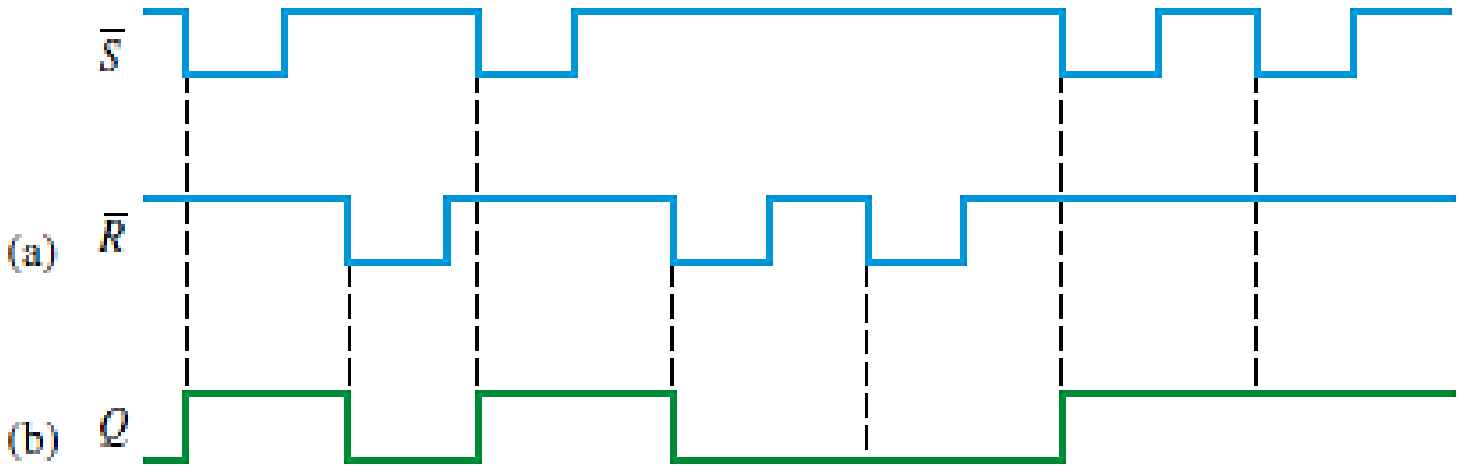


FIGURE 5

Solution

See Figure 5(b).

The Gated S-R Latch

- A gated latch requires an enable input, EN (G is also used to designate an enable input).
- The logic diagram and logic symbol for a gated S-R latch are shown in Figure 8.
- The S and R inputs control the state to which the latch will go when a HIGH level is applied to the EN input.

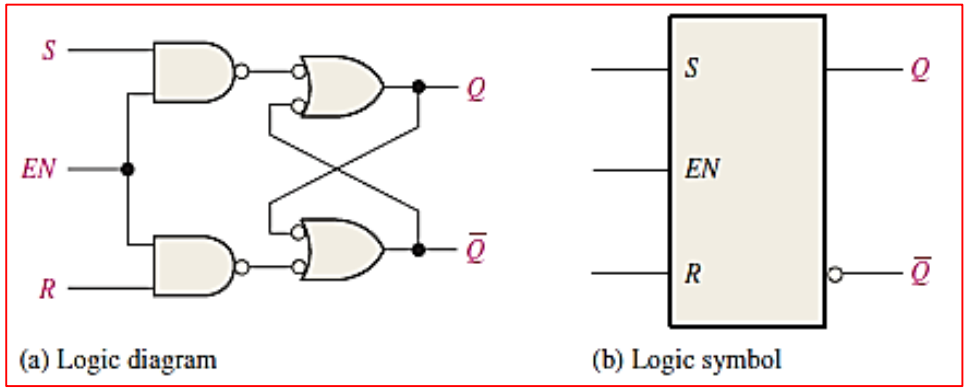


FIGURE 8 A gated S-R latch.

- The latch will not change until EN is HIGH; but as long as it remains HIGH, the output is controlled by the state of the S and R inputs.
- The gated latch is a level-sensitive device. In this circuit, the invalid state occurs when both S and R are simultaneously HIGH and EN is also HIGH.

EXAMPLE 2

Determine the Q output waveform if the inputs shown in Figure 9(a) are applied to a gated S-R latch that is initially RESET.

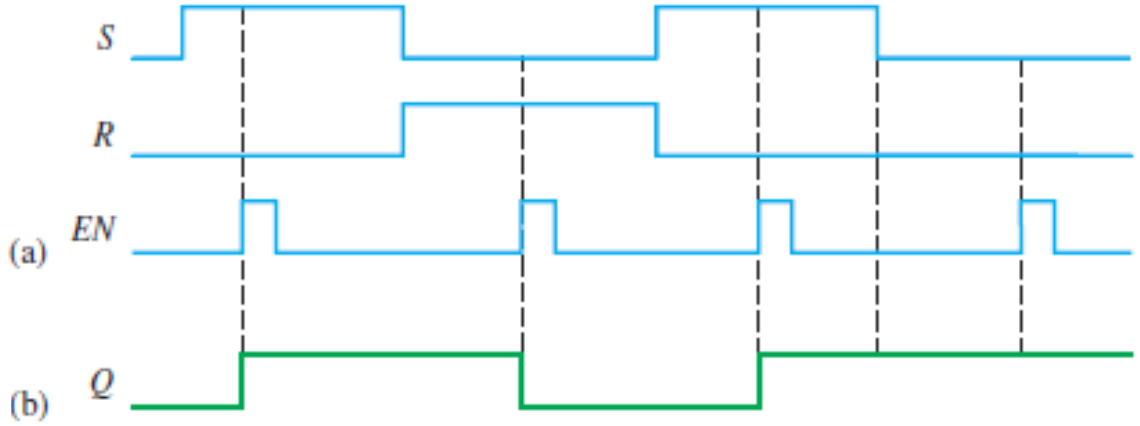


FIGURE 9

Solution

The Q waveform is shown in Figure 9(b). When S is HIGH and R is LOW, a HIGH on the EN input sets the latch. When S is LOW and R is HIGH, a HIGH on the EN input resets the latch. When both S and R are LOW, the Q output does not change from its present state.

Related Problem

Determine the Q output of a gated S-R latch if the S and R inputs in Figure 9(a) are inverted.

The Gated D Latch

- Another type of gated latch is called the D latch. It differs from the S-R latch because it has only one input in addition to EN.
- This input is called the D (data) input. Figure 10 contains a logic diagram and logic symbol of a D latch.
- When the D input is HIGH and the EN input is HIGH, the latch will set.

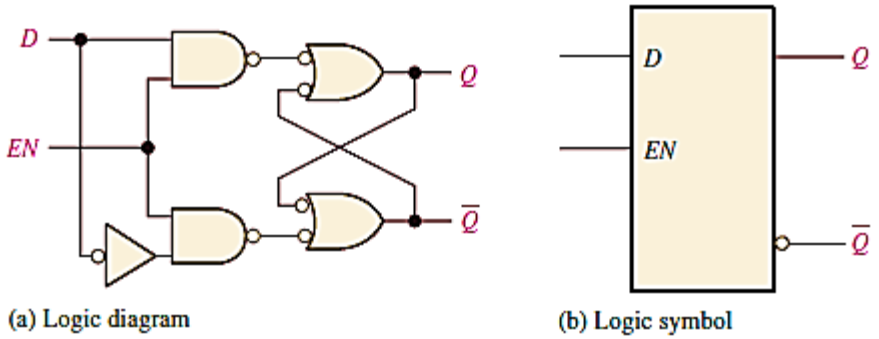


FIGURE 10 A gated D latch.

- When the D input is LOW and EN is HIGH, the latch will reset.
- Stated another way, the output Q follows the input D when EN is HIGH.

EXAMPLE 3

Determine the Q output waveform if the inputs shown in Figure 7–11(a) are applied to a gated D latch, which is initially RESET.

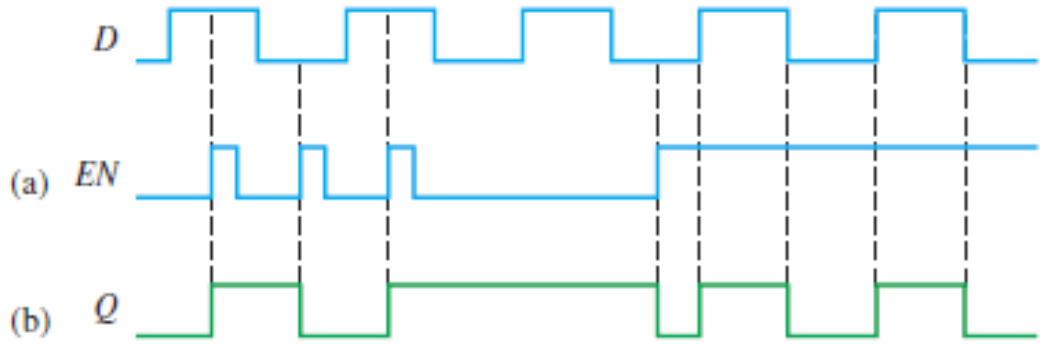


FIGURE 7–11

Solution

The Q waveform is shown in Figure 7–11(b). When D is HIGH and EN is HIGH, Q goes HIGH. When D is LOW and EN i HIGH, Q goes LOW. When EN is LOW, the state of the latch is not affected by the D input.

Related Problem

Determine the Q output of the gated D latch if the D input in Figure 7–11(a) is inverted.

Flip-Flops

- **Flip-flops are synchronous bistable devices, also known as bistable multivibrators.**
- **The term synchronous means that the output changes state only at a specified point (leading or trailing edge) on the triggering input called the clock (CLK), which is designated as a control input, C; that is, changes in the output occur in synchronization with the clock.**
- **Flip-flops are edge-triggered or edge-sensitive whereas gated latches are level-sensitive.**

Edge-triggered flip-flop

- Changes state either at the positive edge (rising edge) or at the negative edge (falling edge) of the clock pulse and is sensitive to its inputs only at this transition of the clock.
- Two types of edge-triggered flip-flops are covered in this section: D and J-K. The logic symbols for these flip-flops are shown in Figure 13.
- Each type can be either positive edge-triggered (no bubble at C input) or negative edge-triggered (bubble at C input).
- The key to identifying an edge-triggered flip-flop by its logic symbol is the small triangle inside the block at the clock (C) input. This triangle is called the dynamic input indicator.

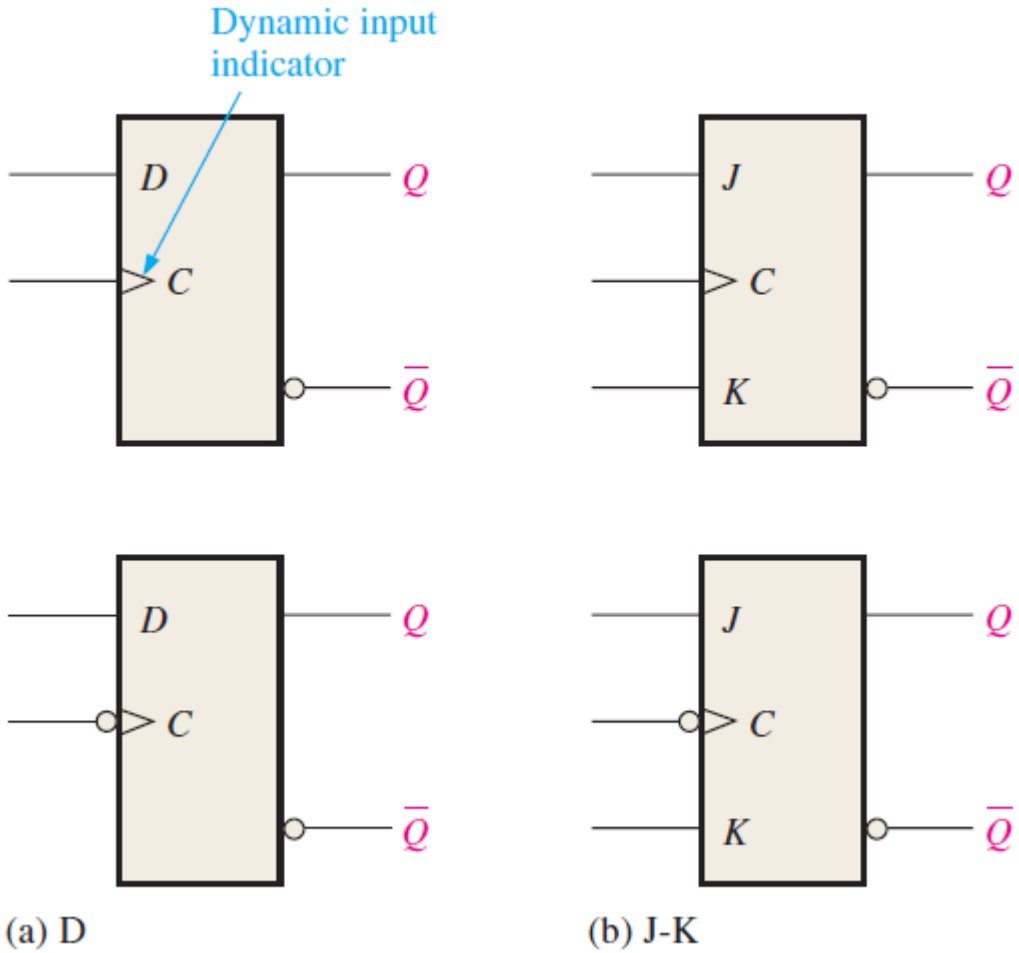
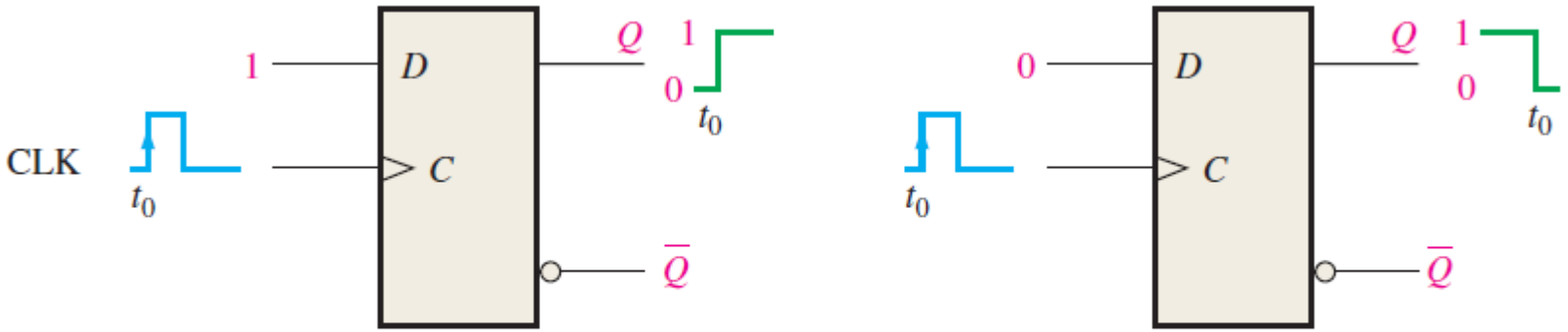


FIGURE 13 Edge-triggered flip-flop logic symbols (top: positive edge-triggered; bottom: negative edge-triggered).

The D Flip-Flop

- The D input of the D flip-flop is a synchronous input because data on the input are transferred to the flip-flop's output only on the triggering edge of the clock pulse.
  - When D is HIGH, the Q output goes HIGH on the triggering edge of the clock pulse, and the flip-flop is SET. When D is LOW, the Q output goes LOW on the triggering edge of the clock pulse, and the flip-flop is RESET.
- This basic operation of a positive edge-triggered D flip-flop is illustrated in Figure 14, and Table 2 is the truth table for this type of flip-flop. Remember, the flip-flop cannot change state except on the triggering edge of a clock pulse. The D input can be changed at any time when the clock input is LOW or HIGH (except for a very short interval around the triggering transition of the clock) without affecting the output. Just remember, Q follows D at the triggering edge of the clock.



(a) $D = 1$ flip-flop SETS on positive clock edge. (If already SET, it remains SET.)

(b) $D = 0$ flip-flop RESETS on positive clock edge. (If already RESET, it remains RESET.)

FIGURE 14
Operation of a positive edge-triggered D flip-flop.

TABLE 2

Truth table for a positive edge-triggered D flip-flop.

Inputs		Outputs		
D	CLK	Q	$\overline{Q}$	Comments
0	↑	0	1	RESET
1	↑	1	0	SET

↑ = clock transition LOW to HIGH

- **The operation and truth table for a negative edge-triggered D flip-flop are the same as those for a positive edge-triggered device except that the falling edge of the clock pulse is the triggering edge.**

EXAMPLE 4

Determine the Q and $\overline{Q}$ output waveforms of the flip-flop in Figure -15 for the D and CLK inputs in Figure 1 -16(a). Assume that the positive edge-triggered flip-flop is initially RESET.

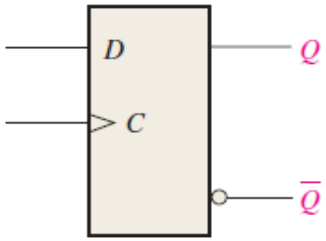


FIGURE 15

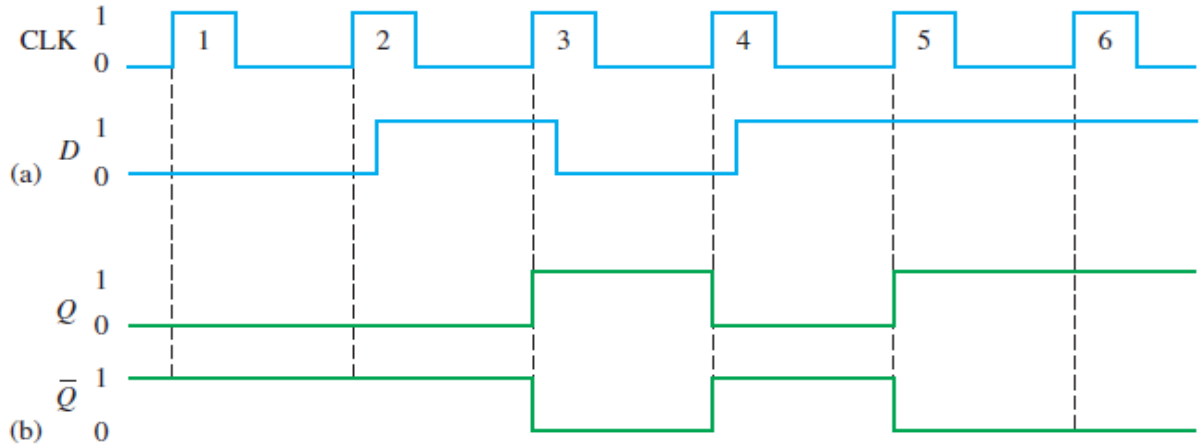


FIGURE 16

Solution

1. At clock pulse 1, D is LOW, so Q remains LOW (RESET).
2. At clock pulse 2, D is LOW, so Q remains LOW (RESET).
3. At clock pulse 3, D is HIGH, so Q goes HIGH (SET).
4. At clock pulse 4, D is LOW, so Q goes LOW (RESET).
5. At clock pulse 5, D is HIGH, so Q goes HIGH (SET).
6. At clock pulse 6, D is HIGH, so Q remains HIGH (SET).

Once Q is determined, $\overline{Q}$ is easily found since it is simply the complement of Q. The resulting waveforms for Q and $\overline{Q}$ are shown in Figure 16(b) for the input waveforms in part (a).

Related Problem

Determine Q and $\overline{Q}$ for the D input in Figure -16(a) if the flip-flop is a negative edge-triggered device.

The J-K Flip-Flop

- The J and K inputs of the J-K flip-flop are synchronous inputs because data on these inputs are transferred to the flip-flop's output only on the triggering edge of the clock pulse
- When J is HIGH and K is LOW, the Q output goes HIGH on the triggering edge of the clock pulse, and the flip-flop is SET.
- When J is LOW and K is HIGH, the Q output goes LOW on the triggering edge of the clock pulse, and the flip-flop is RESET.
- When both J and K are LOW, the output does not change from its prior state.
- When J and K are both HIGH, the flip-flop changes state. This called the toggle mode.
- This basic operation of a positive edge-triggered flip-flop is illustrated in Figure 17, and Table 3 is the truth table for this type of flip-flop.
- The flip-flop cannot change state except on the triggering edge of a clock pulse.
- The J and K inputs can be changed at any time when the clock input is LOW or HIGH (except for a very short interval around the triggering transition of the clock) without affecting the output.

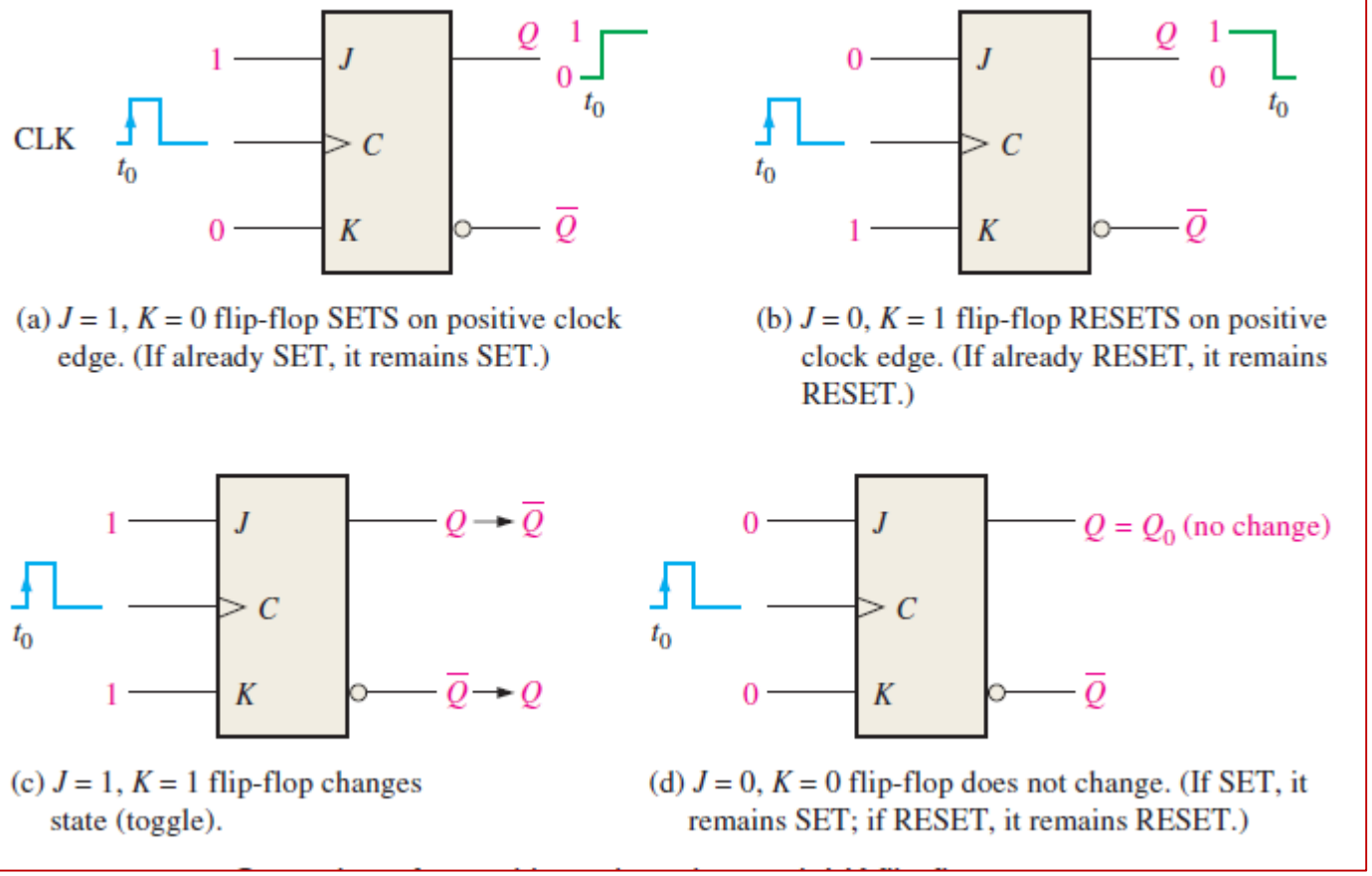


TABLE 3

Truth table for a positive edge-triggered J-K flip-flop.

Inputs			Outputs		
J	K	CLK	Q	$\overline{Q}$	Comments
0	0	↑	Q_0	$\overline{Q}_0$	No change
0	1	↑	0	1	RESET
1	0	↑	1	0	SET
1	1	↑	$\overline{Q}_0$	Q_0	Toggle

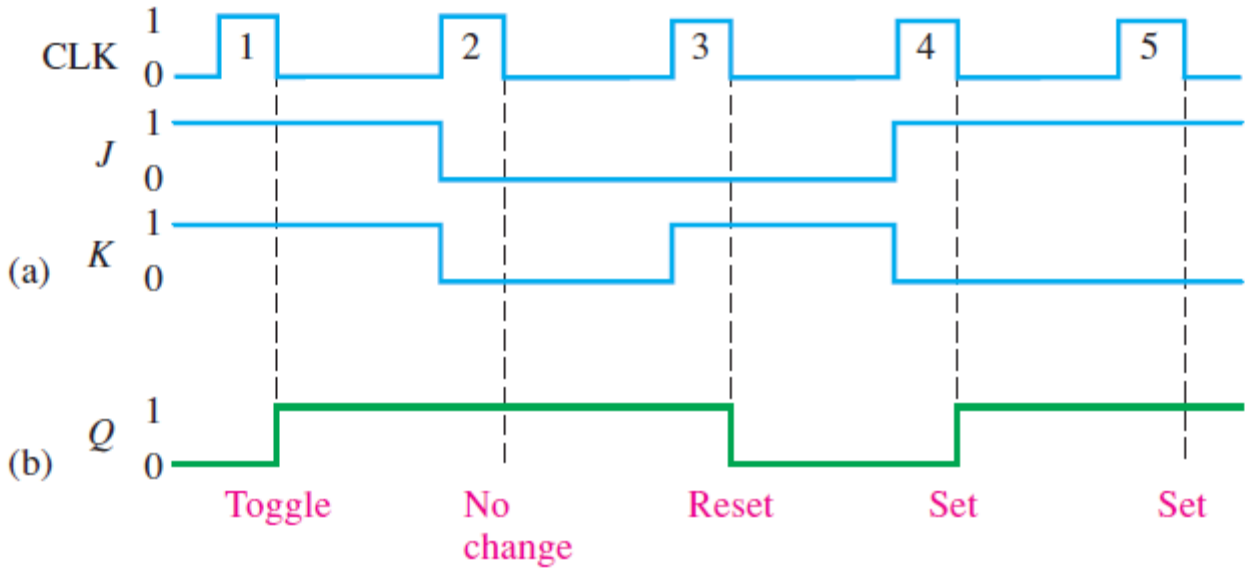
↑ = clock transition LOW to HIGH

Q_0 = output level prior to clock transition

FIGURE 17 Operation of a positive edge-triggered J-K flip-flop.

EXAMPLE 7–5

The waveforms in Figure 18(a) are applied to the J, K, and clock inputs as indicated. Determine the Q output, assuming that the flip-flop is initially RESET.



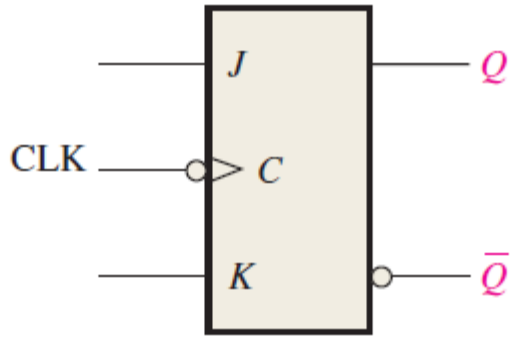


FIGURE 18

Solution

Since this is a negative edge-triggered flip-flop, as indicated by the "bubble" at the clock input, the Q output will change only on the negative-going edge of the clock pulse.

1. At the first clock pulse, both J and K are HIGH; and because this is a toggle condition, Q goes HIGH.
2. At clock pulse 2, a no-change condition exists on the inputs, keeping Q at a HIGH level.
3. When clock pulse 3 occurs, J is LOW and K is HIGH, resulting in a RESET condition; Q goes LOW.
4. At clock pulse 4, J is HIGH and K is LOW, resulting in a SET condition; Q goes HIGH.
5. A SET condition still exists on J and K when clock pulse 5 occurs, so Q will remain HIGH.

The resulting Q waveform is indicated in Figure 18(b).

Related Problem

Determine the Q output of the J-K flip-flop if the J and K inputs in Figure 18(a) are inverted.

Edge-Triggered Operation: D Flip-Flop

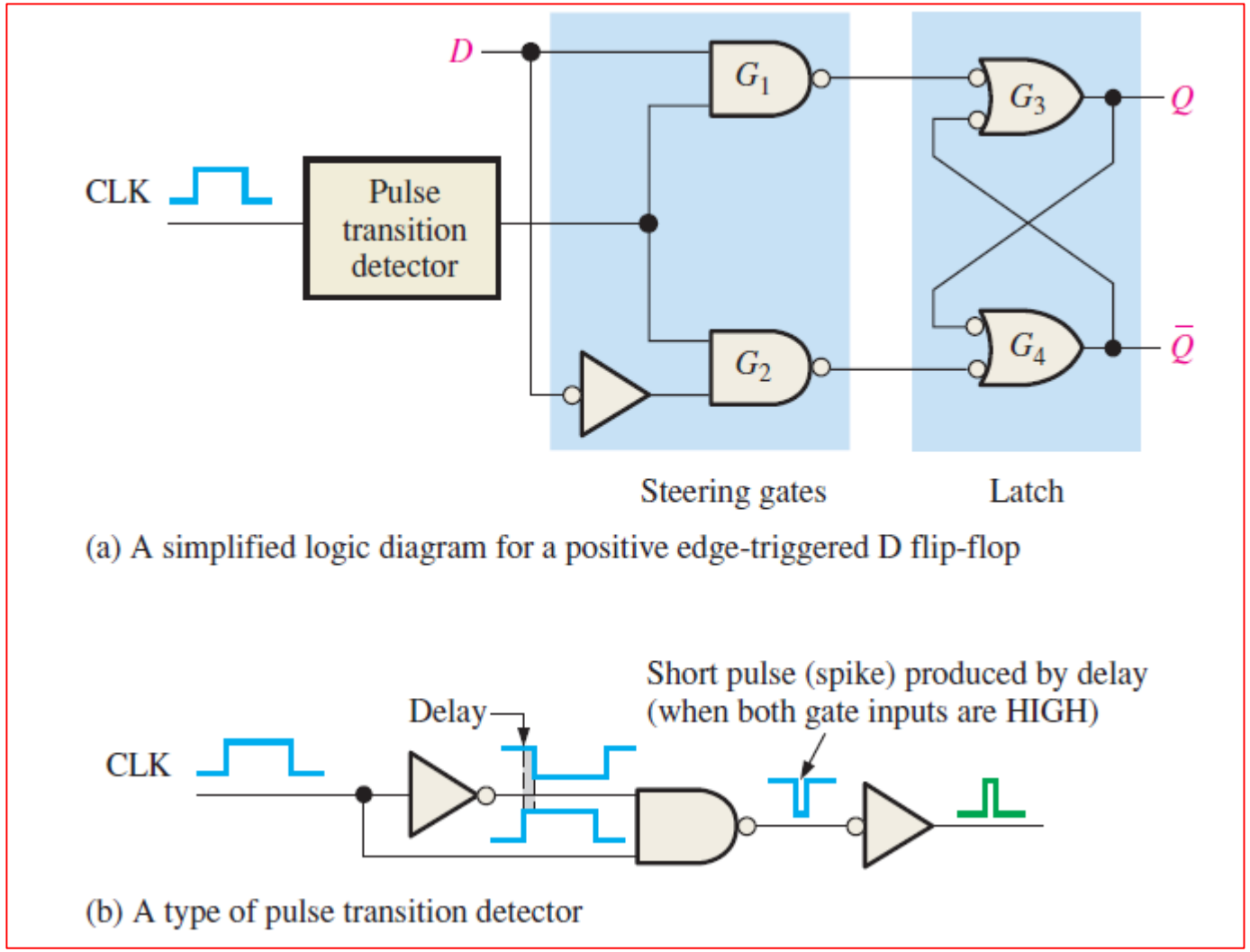


FIGURE 19 Edge triggering.

- **A simplified implementation of an edge-triggered D flip-flop is illustrated in Figure 19(a) and is used to demonstrate the concept of edge-triggering.**
- **Notice that the basic D flip-flop differs from the gated D latch only in that it has a pulse transition detector.**

- **One basic type of pulse transition detector is shown in Figure 19(b).**
  - **There is a small delay through the inverter on one input to the NAND gate so that the inverted clock pulse arrives at the gate input a few nanoseconds after the true clock pulse.**
  - **This circuit produces a very short-duration spike on the positive-going transition of the clock pulse. In a negative edge-triggered flip-flop the clock pulse is inverted first, thus producing a narrow spike on the negative-going edge.**
  - **The circuit in Figure 19(a) is partitioned into two sections, one labeled Steering gates and the other labeled Latch.**
  - **The steering gates direct, or steer, the clock spike either to the input to gate G3 or to the input to gate G4, depending on the state of the D input.**
  - **The RESET state (Q = 0) and that the D and CLK inputs are LOW. For this condition, the outputs of gate G1 and gate G2 are both HIGH. The LOW on the Q output is coupled back into one input of gate G4, making the $\overline{Q}$ output HIGH.**
  - **Both inputs to gate G3 are HIGH (remember, the output of gate G1 is HIGH), holding the Q output LOW. If a pulse is applied to the CLK input, the outputs of gates G1 and G2 remain HIGH because they are disabled by the LOW on the D input; therefore, there is no change in the state of the flip-flop—it remains in the RESET state.**

- When make D HIGH and apply a clock pulse.
- Because the D input to gate G1 is now HIGH, the output of gate G1 goes LOW for a very short time (spike) when CLK goes HIGH, causing the Q output to go HIGH.
- Both inputs to gate G4 are now HIGH (remember, gate G2 output is HIGH because D is HIGH), forcing the $\overline{Q}$ output LOW.
- This LOW on $\overline{Q}$ is coupled back into one input of gate G3, ensuring that the Q output will remain HIGH.
- The flip-flop is now in the SET state. Figure 20 illustrates the logic level transitions that take place within the flip-flop for this condition.

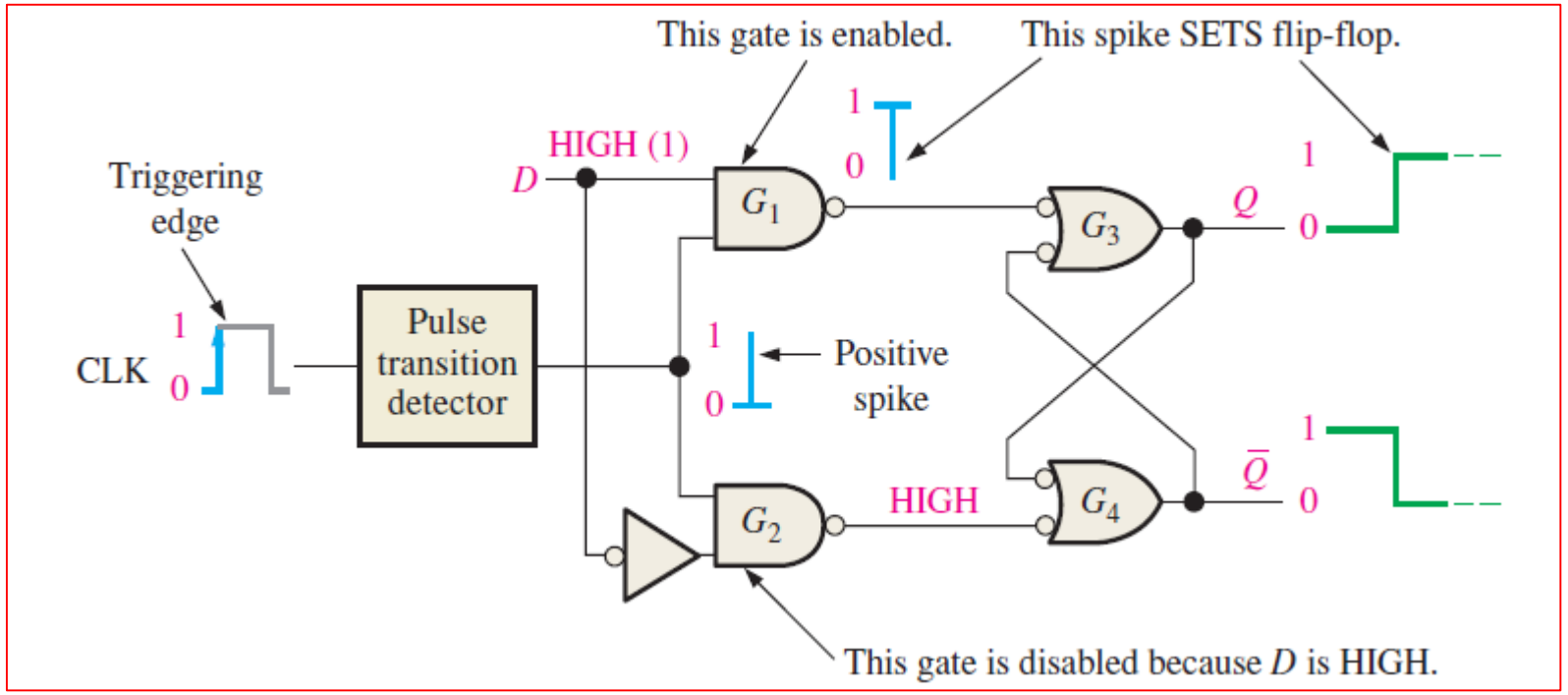


FIGURE 20 Flip-flop making a transition from the RESET to the SET on the positive-going edge of the clock pulse.

When D LOW and apply a clock pulse.

- **The positive-going edge of the clock produces a negative-going spike on the output of gate G2, causing the $\overline{Q}$ output to go HIGH.**
- **Because of this HIGH on $\overline{Q}$, both inputs to gate G3 are now HIGH (remember, the output of gate G1 is HIGH because of the LOW on D), forcing the Q output to go LOW.**
- **This LOW on Q is coupled back into one input of gate G4, ensuring that $\overline{Q}$ will remain HIGH. The flip-flop is now in the RESET state. Figure 21 illustrates the logic level transitions that occur within the flip-flop for this condition.**

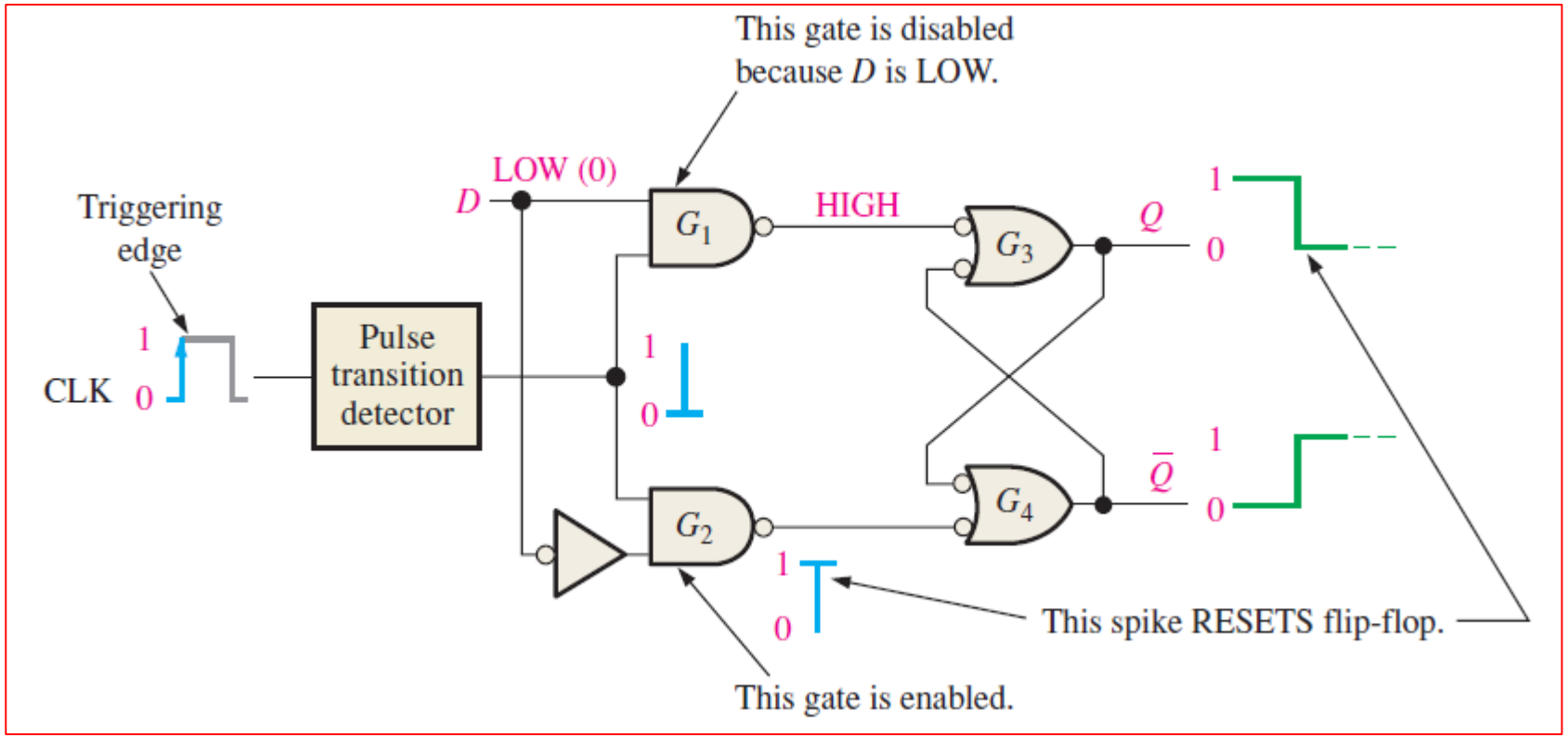


FIGURE 21 Flip-flop making a transition from the SET to the RESET on the positive-going edge of the clock pulse.

EXAMPLE 6

Given the waveforms in Figure 22(a) for the D input and the clock, determine the Q output waveform if the flip-flop starts out RESET.

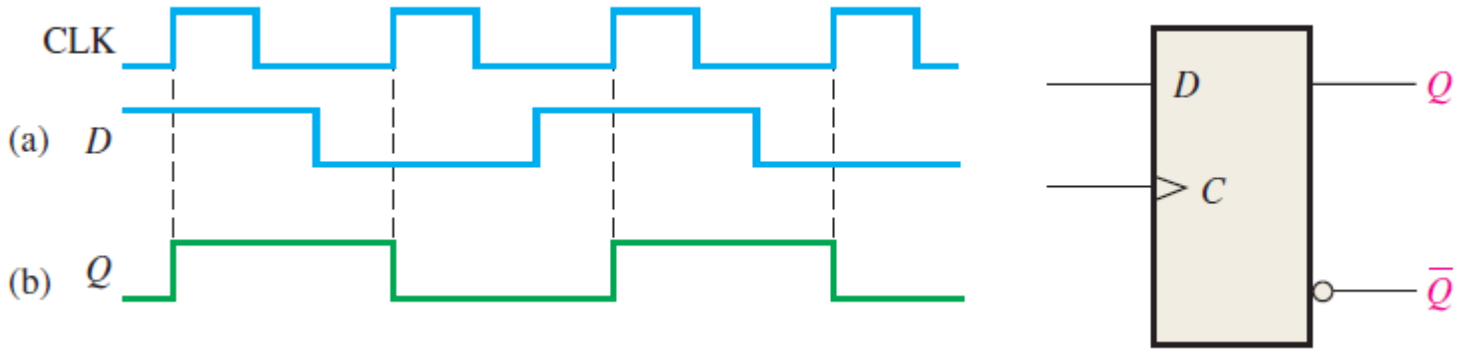


FIGURE 22

Solution

The Q output goes to the state of the D input at the time of the positive-going clock edge. The resulting output is shown in Figure 22(b).

Related Problem

Determine the Q output for the D flip-flop if the D input in Figure 22(a) is inverted.

J-K Flip-Flop

- Figure 23 shows the basic internal logic for a positive edge-triggered J-K flip-flop.
- The Q output is connected back to the input of gate G2, and the Q output is connected back to the input of gate G1.
- The two control inputs are labeled J and K in honor of Jack Kilby, who invented the integrated circuit.
- J-K flip-flop can also be of the negative edge-triggered type, in which case the clock input is inverted.

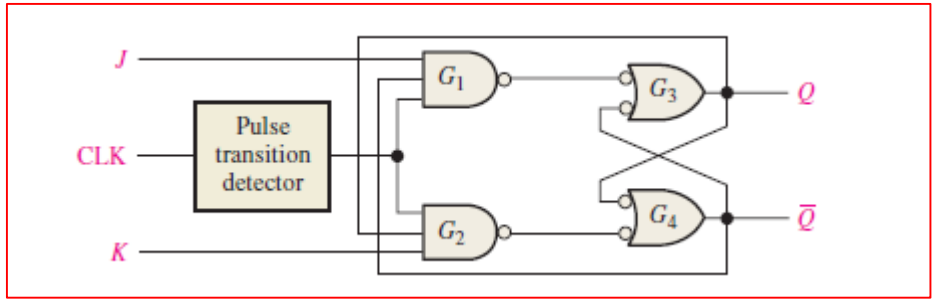


FIGURE 23 A simplified logic diagram for a positive edge-triggered J-K flip-flop.

- Assume that the flip-flop in Figure 24 is RESET and that the J input is HIGH and the K input is LOW rather than as shown.
- When a clock pulse occurs, a leading-edge spike indicated by ① is passed through gate G1 because $\overline{Q}$ s HIGH and J is HIGH.
- This will cause the latch portion of the flip-flop to change to the SET state. The flip-flop is now SET.

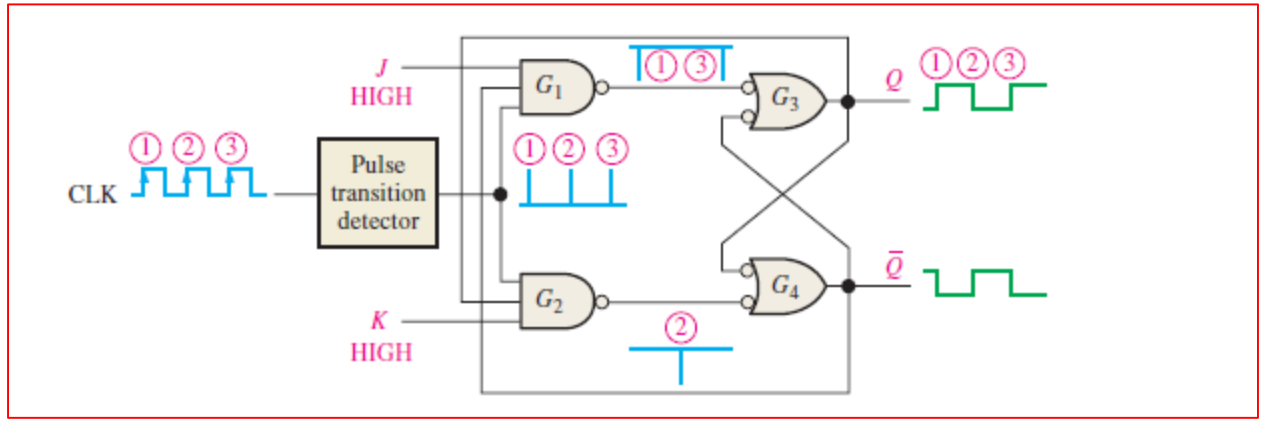


FIGURE 24 Transitions illustrating flip-flop operation.

In the toggle mode, a J-K flip-flop changes state on every clock pulse.

- When J LOW and K HIGH, the next clock spike indicated by ② will pass through gate G2 because Q is HIGH and K is HIGH.
- This will cause the latch portion of the flip-flop to change to the RESET state.

- Applying a LOW to both the J and K inputs, the flip-flop will stay in its present state when a clock pulse occurs.
- A LOW on both J and K results in a no-change condition.

- When both the J and K inputs are HIGH and the flip-flop is RESET, the HIGH on the $\overline{Q}$ enables gate G1; so the clock spike indicated by ③ passes through to set the flip-flop.

- Now there is a HIGH on Q, which allows the next clock spike to pass through gate G2 and reset the flip-flop.

- As you can see, on each successive clock spike, the flip-flop toggles to the opposite state. Figure 24 illustrates the transitions when the flip-flop is in the toggle mode. A J-K flip-flop connected for toggle operation is sometimes called a T flip-flop.

Asynchronous Preset and Clear Inputs

An active preset input makes the Q output HIGH (SET).

- For the flip-flops just discussed, the D and J-K inputs are called synchronous inputs because data on these inputs are transferred to the flip-flop's output only on the triggering edge of the clock pulse; that is, the data are transferred synchronously with the clock.

- Most integrated circuit flip-flops also have asynchronous inputs. These are inputs that affect the state of the flip-flop independent of the clock.

- They are normally labeled preset (PRE) and clear (CLR), or direct set (SD) and direct reset (RD) by some manufacturers.
- An active level on the preset input will set the flip-flop, and an active level on the clear input will reset it.

An active clear input makes the *Q* output LOW (RESET).

- A logic symbol for a D flip-flop with preset and clear inputs is shown in Figure 25. These inputs are active-LOW, as indicated by the bubbles.

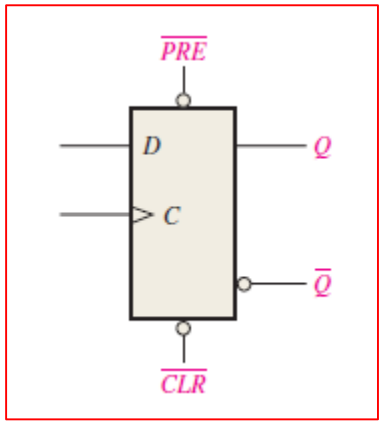


FIGURE 25 Logic symbol for a D flip-flop with active-LOW preset and clear inputs.

- These preset and clear inputs must both be kept HIGH for synchronous operation. In normal operation, preset and clear would not be LOW at the same time.
- Figure 26 shows the logic diagram for an edge-triggered D flip-flop with active-LOW preset ($\overline{PRE}$) and clear ($\overline{\boldsymbol{CLR}}$) inputs.
- This figure illustrates basically how these inputs work. As you can see, they are connected so that they override the effect of the synchronous input, D and the clock.

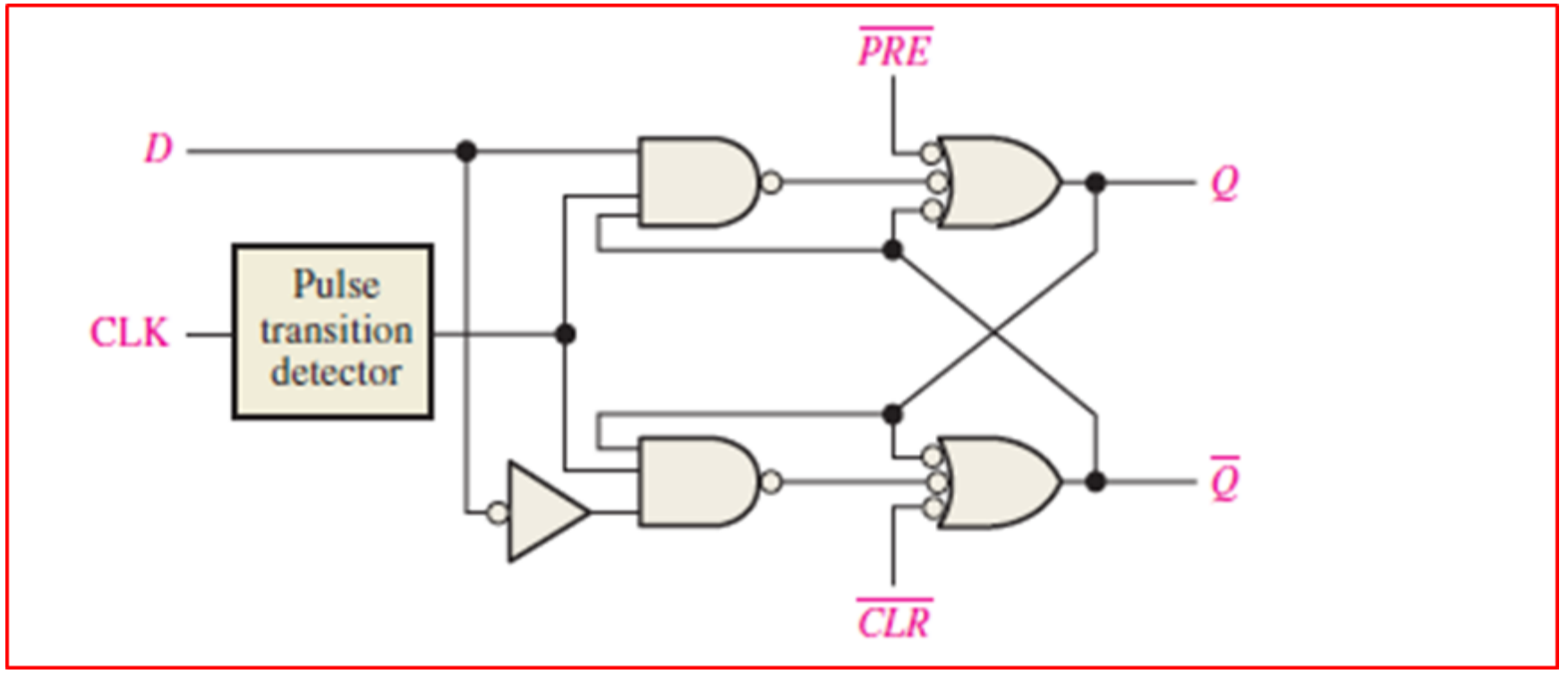
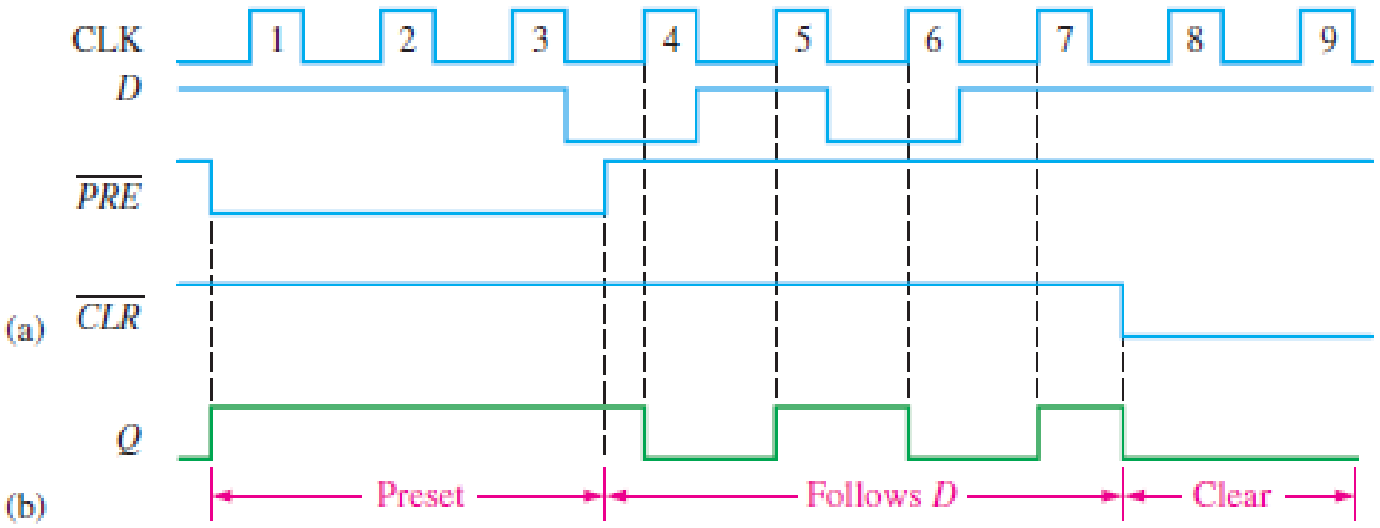


FIGURE 26 Logic diagram for a basic D flip-flop with active-LOW preset and clear inputs.

EXAMPLE 7

For the positive edge-triggered D flip-flop with preset and clear inputs in Figure 27, determine the Q output for the inputs shown in the timing diagram in part (a) if Q is initially LOW.



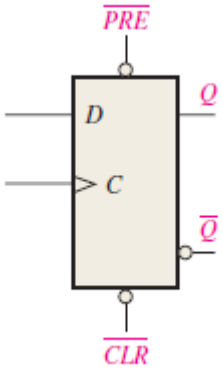


FIGURE 27

Solution

1. During clock pulses 1, 2, and 3, the preset ($\overline{PRE}$) is LOW, keeping the flip-flop SET regardless of the synchronous D input.
2. For clock pulses 4, 5, 6, and 7, the output follows the input on the clock pulse because both $\overline{PRE}$ and $\overline{CLR}$ are HIGH.
3. For clock pulses 8 and 9, the clear ($\overline{CLR}$) input is LOW, keeping the flip-flop RESET regardless of the synchronous inputs.

The resulting Q output is shown in Figure 27(b).

Related Problem

If you interchange the $\overline{PRE}$ and $\overline{CLR}$ waveforms in Figure 27(a), what will the Q output look like?

FLIP-Flop Operating Characteristics

❖ Propagation Delay Times

- A propagation delay time is the interval of time required after an input signal has been applied for the resulting output change to occur. Four categories of propagation delay times are important in the operation of a flip-flop:
  - 1. Propagation delay t_{PLH} as measured from the triggering edge of the clock pulse to the LOW-to-HIGH transition of the output. This delay is illustrated in Figure 31(a).
  - 2. Propagation delay t_{PHL} as measured from the triggering edge of the clock pulse to the HIGH-to-LOW transition of the output. This delay is illustrated in Figure 31(b).

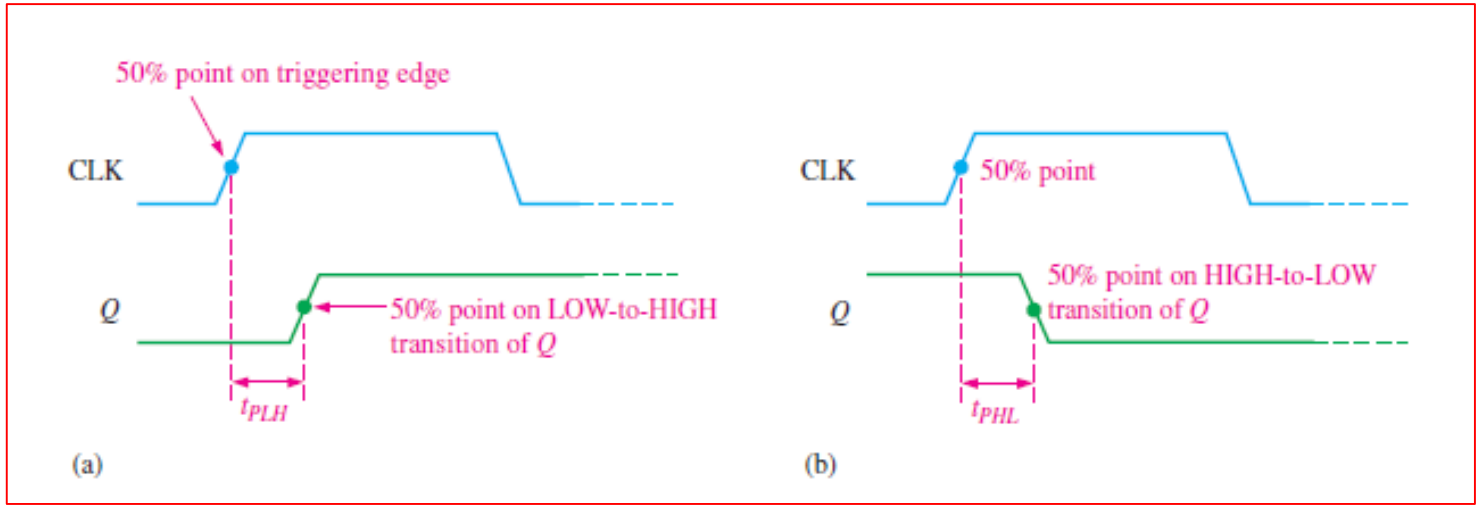


FIGURE 31 Propagation delays, clock to output

- 3. Propagation delay t_{PLH} as measured from the leading edge of the preset input to the
- LOW-to-HIGH transition of the output. This delay is illustrated in Figure 32(a)
- for an active-LOW preset input.

- 4. Propagation delay t_{PHL} as measured from the leading edge of the clear input to the
- HIGH-to-LOW transition of the output. This delay is illustrated in Figure 32(b)
- for an active-LOW clear input.

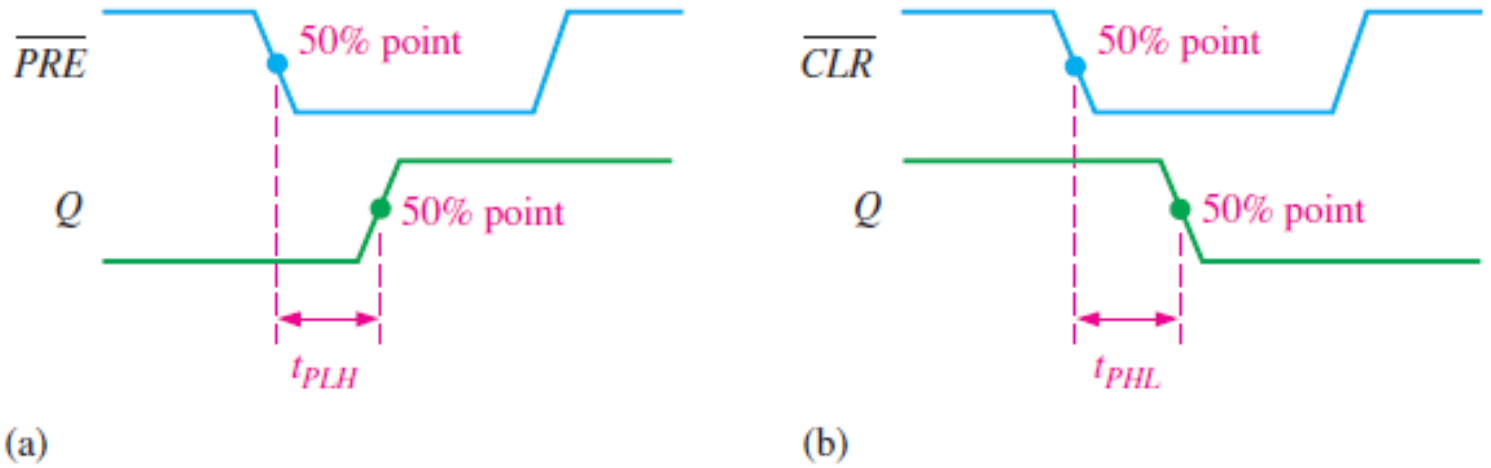


FIGURE 32 Propagation delays, preset input to output and clear input to output.

❖ Set-up Time

The set-up time (t_s) is the minimum interval required for the logic levels to be maintained constantly on the inputs (J and K, or D) prior to the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip flop. This interval is illustrated in Figure (33) for a D flip-flop.

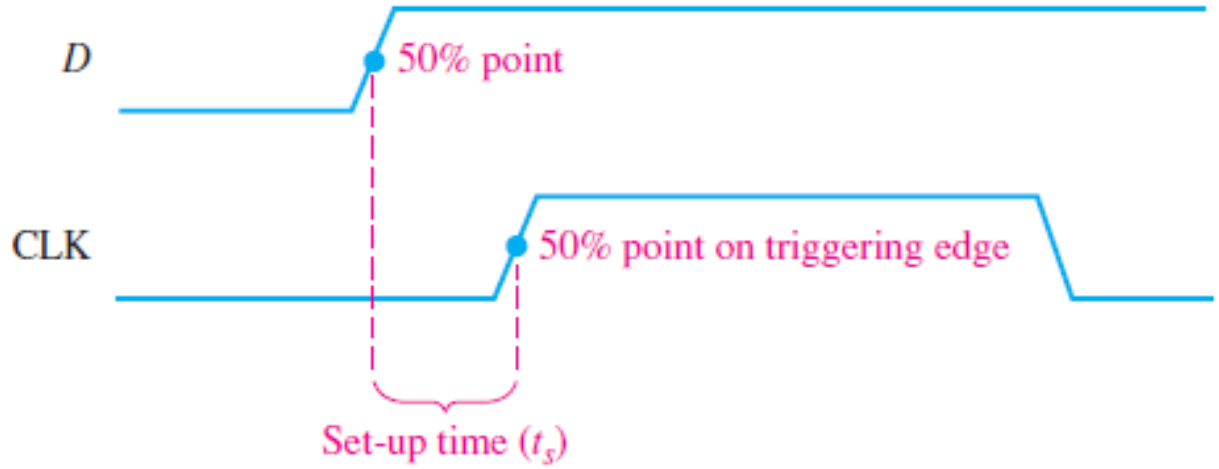


FIGURE 33 Set-up time ($\boldsymbol{t_s}$). The logic level must be present on the D input for a time equal to or greater than ts before the triggering edge of the clock pulse for reliable data entry.

❖ Hold Time

The hold time (t_h) is the minimum interval required for the logic levels to remain on the inputs after the triggering edge of the clock pulse in order for the levels to be reliably clocked into the flip-flop. This is illustrated in Figure 34 for a D flip-flop.

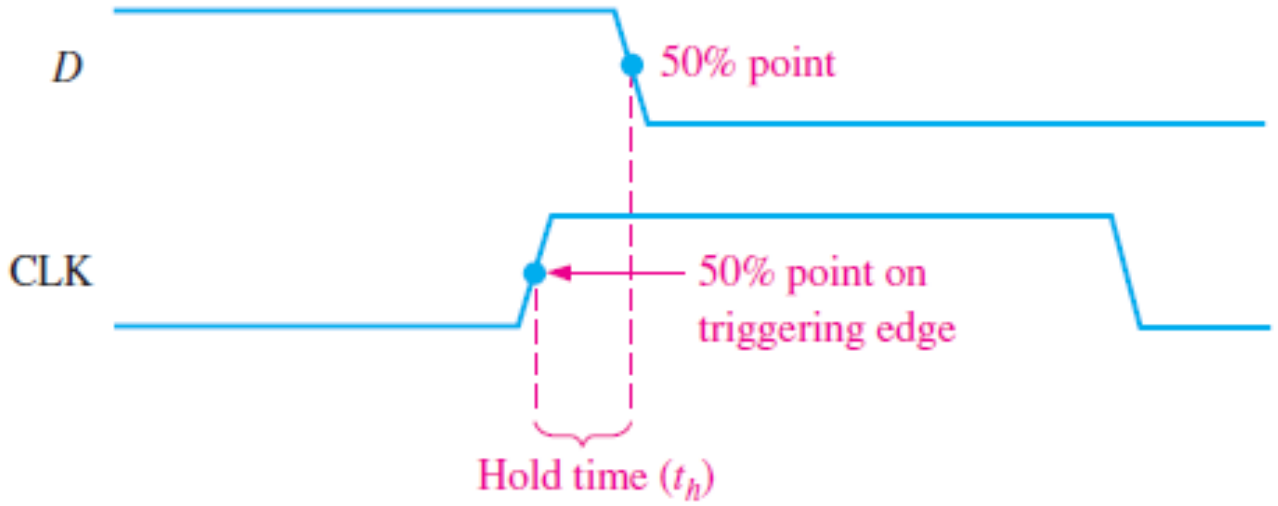


FIGURE 34 Hold time ($\boldsymbol{t_h}$). The logic level must remain on the D input for a time equal to or greater than th after the triggering edge of the clock pulse for reliable data entry.

❖ **Maximum Clock Frequency**

The maximum clock frequency (f_{max}) is the highest rate at which a flip-flop can be reliably triggered. At clock frequencies above the maximum, the flip-flop would be unable to respond quickly enough, and its operation would be impaired.

❖ **Pulse Widths**

Minimum pulse widths (t_W) for reliable operation are usually specified by the manufacturer for the clock, preset, and clear inputs. Typically, the clock is specified by its minimum HIGH time and its minimum LOW time.

❖ **Power Dissipation**

The **power dissipation** of any digital circuit is the total power consumption of the device. For example, if the flip-flop operates on a +5 V dc source and draws 5 mA of current, the power dissipation is

$$P = V_{CC} * I_{CC} = 5\ V * 5\ mA = 25\ mW$$

The power dissipation is very important in most applications in which the capacity of the dc supply is a concern. As an example, let's assume that you have a digital system that requires a total of ten flip-flops, and each flip-flop dissipates 25 mW of power. The total power requirement is

$$PT = 10 * 25\ mW = 250\ mW = 0.25\ W$$

This tells you the output capacity required of the dc supply. If the flip-flops operate on +5 V dc, then the amount of current that the supply must provide is

$$\mathbf{I = \frac{250\ mW}{5\ V} = 50\ mA}$$

You must use a +5 V dc supply that is capable of providing at least 50 mA of current.

Flip-Flop Applications

❖ Parallel Data Storage

- A common requirement in digital systems is to store several bits of data from parallel lines simultaneously in a group of flip-flops.
- This operation is illustrated in Figure 35(a) using four flip-flops. Each of the four parallel data lines is connected to the *D* input of a flip-flop.
- The clock inputs of the flip-flops are connected together, so that each flip-flop is triggered by the same clock pulse.
- In this example, positive edge-triggered flip-flops are used, so the data on the D inputs are stored simultaneously by the flip-flops on the positive edge of the clock, as indicated in the timing diagram in Figure 35(b).
  - Also, the asynchronous reset (R) inputs are connected to a common $\overline{CLR}$ line, which initially resets all the flip-flops.
- This group of four flip-flops is an example of a basic register used for data storage. In digital systems, data are normally stored in groups of bits (usually eight or multiples thereof) that represent numbers, codes, or other information.

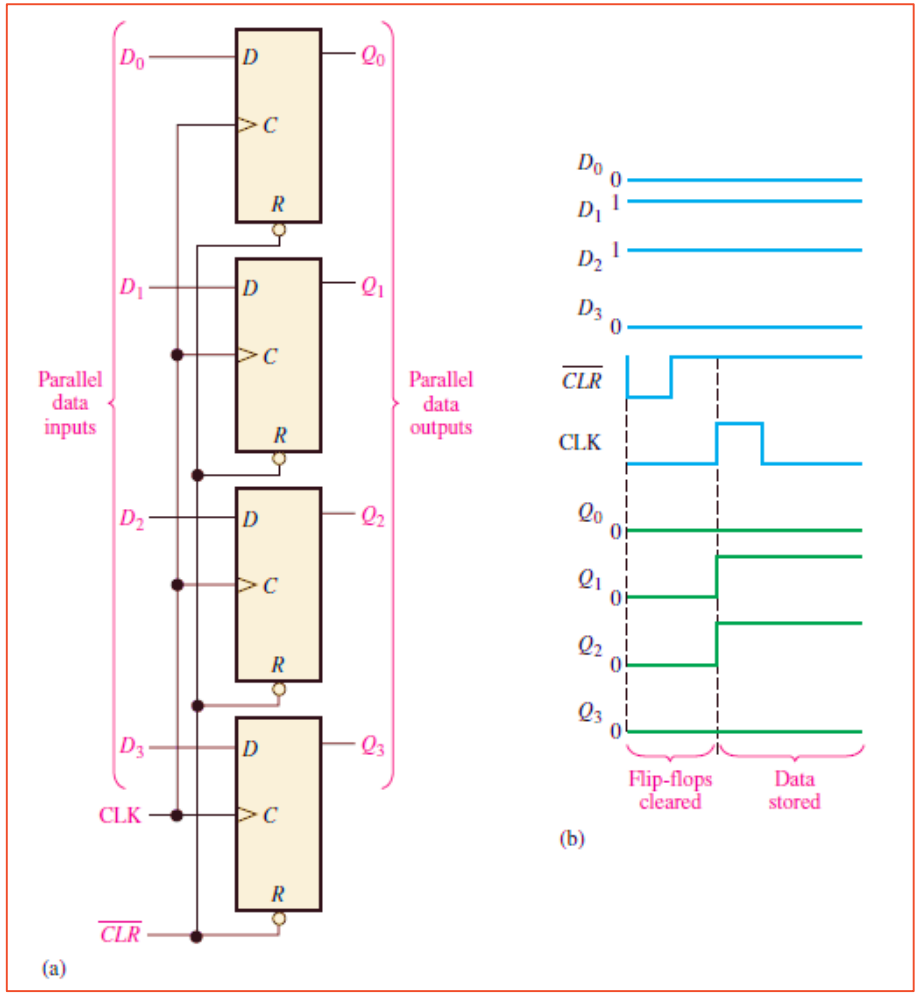


FIGURE 35 Example of flip-flops used in a basic register for parallel data storage.

❖ Frequency Division

- Another application of a flip-flop is dividing (reducing) the frequency of a periodic waveform.
- When a pulse waveform is applied to the clock input of a D or J-K flip-flop that is connected to toggle (D = $\bar{Q}$ or J = K = 1), the Q output is a square wave with one-half the frequency of the clock input.
- Thus, a single flip-flop can be applied as a divide-by-2 device, as is illustrated in Figure 36 for both a D and a J-K flip-flop. As you can see in part (c), the flip-flop changes state on each triggering clock edge (positive edge-triggered in this case).
- This results in an output that changes at half the frequency of the clock waveform.

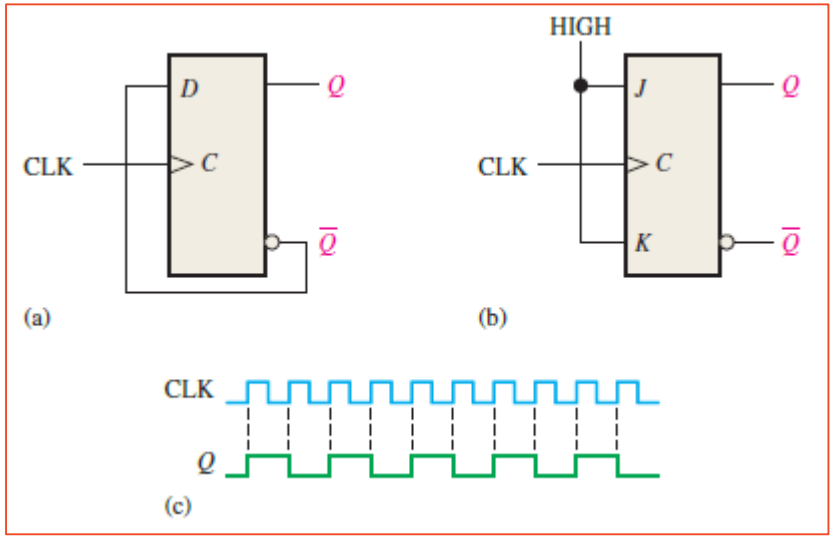


FIGURE 36 The D flip-flop and J-K flip-flop as a divide-by-2 device. Q is one-half the frequency of CLK.

- Further division of a clock frequency can be achieved by using the output of one flipflop as the clock input to a second flip-flop, as shown in Figure 37.

The frequency of the Q_A output is divided by 2 by flip-flop B. The Q_B output is, therefore, one-fourth the frequency of the original clock input.

- Propagation delay times are not shown on the timing diagrams. By connecting flip-flops in this way, a frequency division of 2^n is achieved, where n is the number of flip-flops.
- For example, three flip-flops divide the clock frequency by 2^3 = 8; four flip-flops divide the clock frequency by 2^4 = 16; and so on.

EXAMPLE 9

Develop the fout waveform for the circuit in Figure 38 when an 8 kHz square wave input is applied to the clock input of flip-flop A.

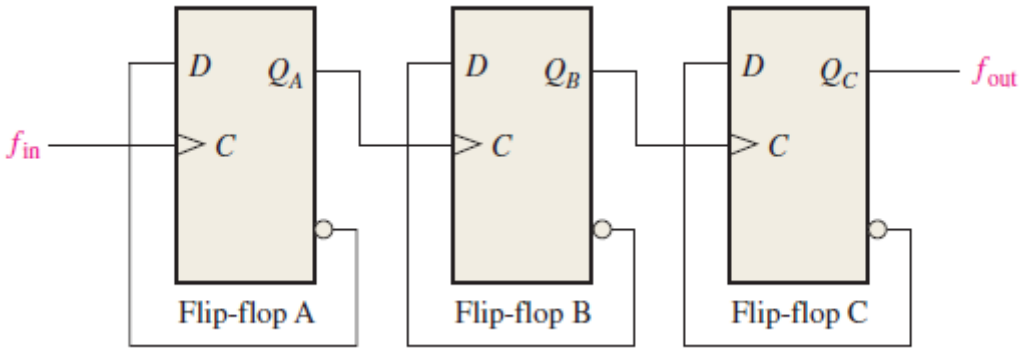


Figure 38

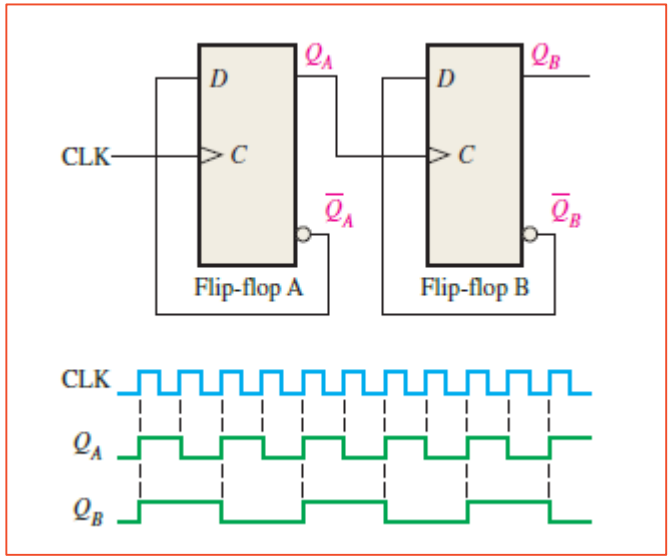


FIGURE 37 Example of two D flip-flops used to divide the clock frequency by 4. QA is one-half and QB is one-fourth the frequency of CLK.

Solution

The three flip-flops are connected to divide the input frequency by eight (2^3 = 8) and thef_{out}(f_{out}) waveform is shown in Figure 7–39. Since these are positive edge-triggered flip-flops, the outputs change on the positive-going clock edge. There is one output pulse for every eight input pulses, so the output frequency is 1 kHz. Waveforms of $Q_A$and Q_B are also shown.

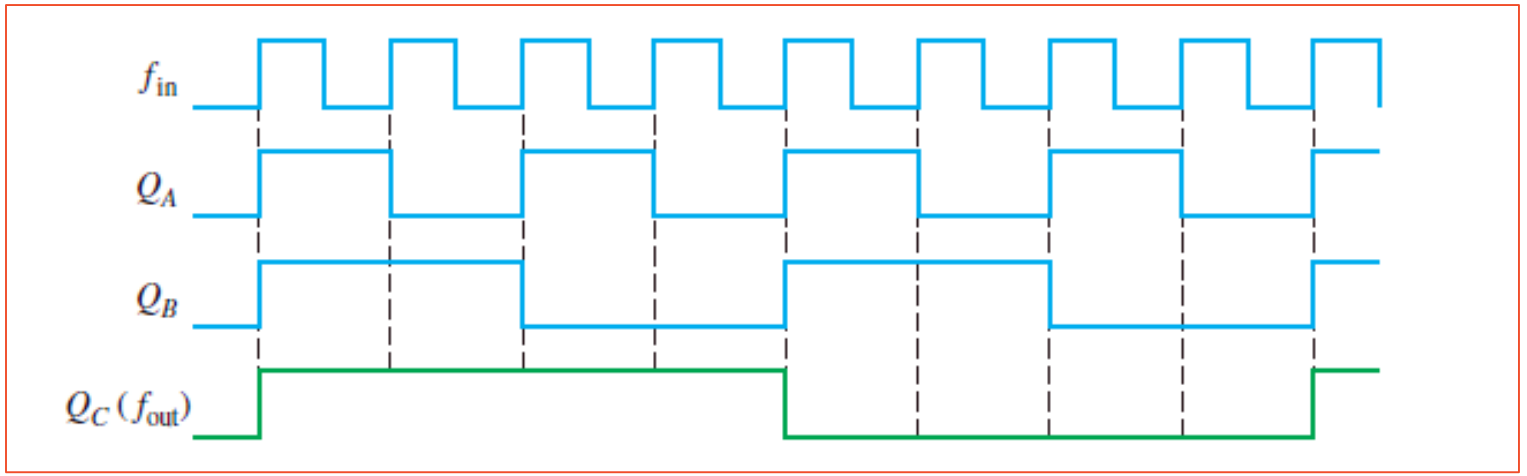


FIGURE 39

❖ Counting

- Another important application of flip-flops is in digital counters
- The concept is illustrated in Figure 40. Negative edge-triggered J-K flip-flops are used for illustration. Both flip-flops are initially RESET. Flip-flop A toggles on the negative-going transition of each clock pulse.
- The Q output of flip-flop A clocks flip-flop B, so each time $Q_A$makes a HIGH-to-LOW transition, flip-flop B toggles. The resulting Q_A and Q_B waveforms are shown in the figure.
- Observe the sequence of Q_A and $Q_B$in Figure 40. Prior to clock pulse 1, Q_A = 0 and Q_B = 0; after clock pulse 1, Q_A = 1 and Q_B = 0; after clock pulse 2, Q_A = 0 and Q_B = 1; and after clock pulse 3, Q_A = 1 and Q_B = 1.

- If we take Q_A as the least significant bit, a 2-bit sequence is produced as the flip-flops are clocked.
- This binary sequence repeats every four clock pulses, as shown in the timing diagram of Figure 40.
- Thus, the flip-flops are counting in sequence from 0 to 3 (00, 01, 10, 11) and then recycling back to 0 to begin the sequence again.

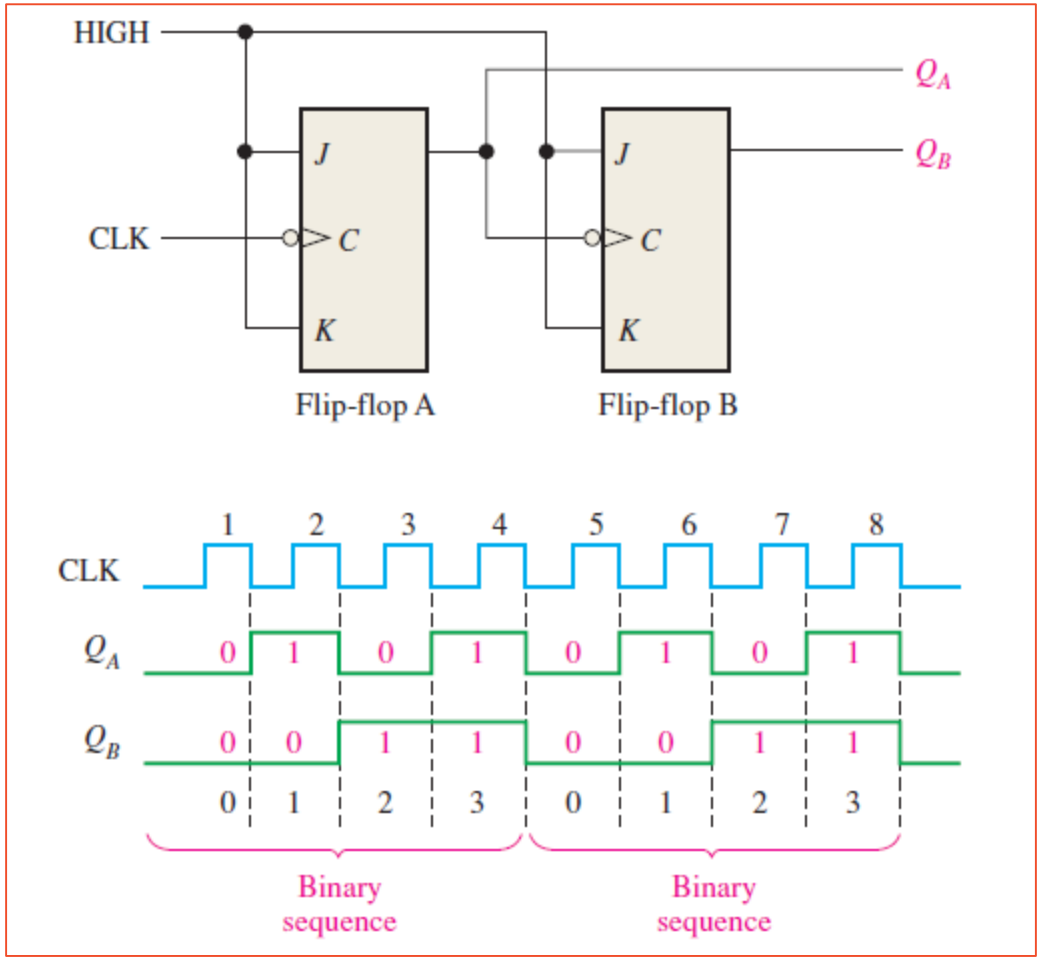


FIGURE 40 J-K flip-flops used to generate a binary count sequence (00, 01, 10, 11). Two repetitions are shown.

EXAMPLE 10

Determine the output waveforms in relation to the clock for Q_A , Q_B and Q_C in the circuit of Figure 7–41 and show the binary sequence represented by these waveforms.

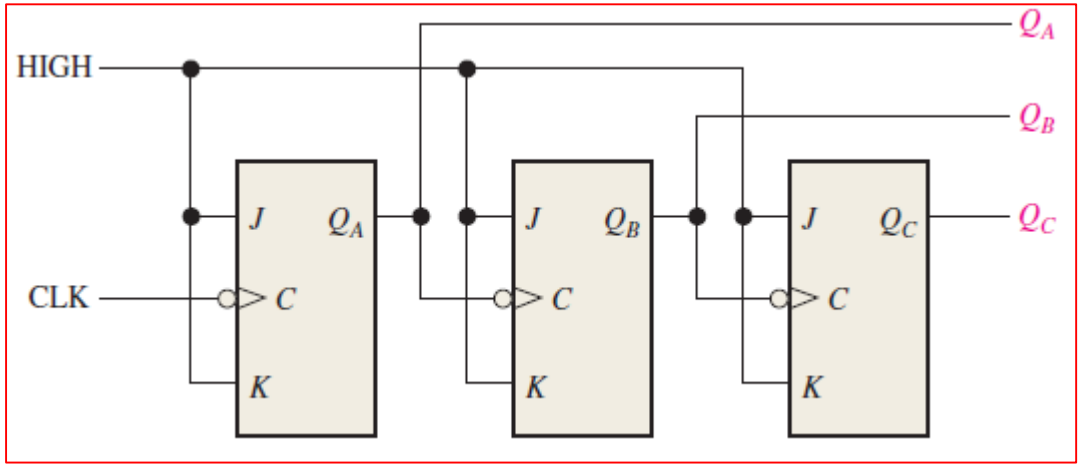


FIGURE 41

Solution

The output timing diagram is shown in Figure 42. Notice that the outputs change on the negative-going edge of the clock pulses. The outputs go through the binary sequence
000, 001, 010, 011, 100, 101, 110, and 111 as indicated.

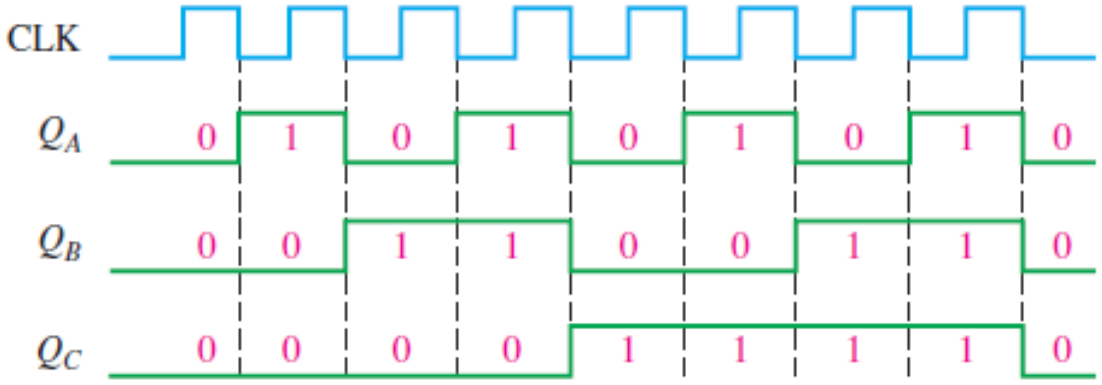


FIGURE 42

Related Problem

How many flip-flops are required to produce a binary sequence representing decimal numbers 0 through 15?