Computer Engineering

Electrical Engineering Department

Third Stage

2nd Semester

Instructor: Asst. Lecturer

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Intel 80286 Microprocessor

- The 80286 microprocessor is an advanced version of the 8086 microprocessor that was designed for multiuser and multitasking environments.
- The 80286 addresses 16M bytes (24 Address lines) of physical memory and 1G bytes of virtual memory by using its memory-management system.
- Intel 80286 is a high performance 16 bit microprocessor unit
- Performance : 6xfaster than 8086 MPU
- 80286 operates with three clock frequencies 12.5 MHz, 10 MHz, and 8 MHz.
- The 80286 operates in both the real mode and protected modes.
- Available in 68 pin IC package.

Hardware Features

- The CPU of the 80286 processor consists of four functional units such as
- Address Unit (AU)
- Bus Unit (BU)
- Instruction Unit (IU)
- Execution Unit (EU)
- **Address Unit (AU):** The AU calculates the physical addresses of instructions and data based on the segment register and a 16-bit offset, similar to the 8086. This unit generates a 20-bit physical address used to address memory and peripheral devices. The computed address is then passed to the Bus Unit (BU).
- **Bus Unit (BU):** The BU interfaces the 80286 with memory and I/O devices through a 16-bit data bus, a 24-bit address bus, and a control bus. It manages all external bus operations, including latching and driving the address bus lines (A19-A0) for memory and I/O read and write processes. The BU is also responsible for instruction prefetching, where instructions are fetched and stored in a 6-byte prefetch queue to speed up execution. This process, known as instruction pipelining, ensures that while one instruction executes, the next instruction is fetched and prepared for immediate use.
- **Instruction Unit (IU):** The IU handles the decoding of fetched instructions and prepares them for execution.
- **Execution Unit (EU):** The EU executes the instructions decoded by the IU, performing the necessary computations and operations. See Fig. 1

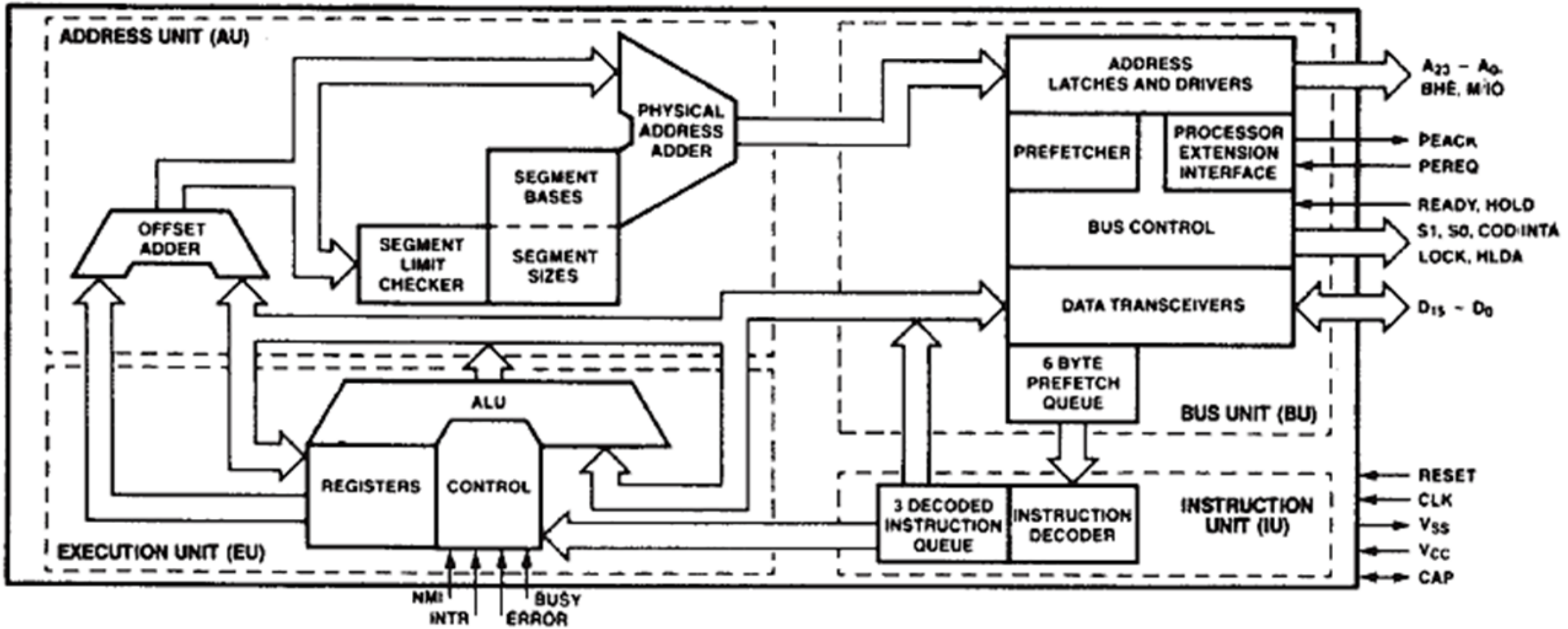

Figure 1. The block diagram of the 80286 microprocessor.

- Figure 1. shows the internal block diagram of the 80286 microprocessor. it contains a memory management unit (MMU) that is called the address unit in the block diagram.

- As a careful examination of the block diagram reveals, address pins A23–A0, $\overline{BUSY}$, CAP, $\overline{ERROR}, \overline{PEREQ}$, and $\overline{PEACK}$ and are new or additional pins that do not appear on the 8086 microprocessor The $\overline{BUSY}$, $\overline{ERROR}, \overline{PEREQ}$, and $\overline{PEACK}$ and signals are used with the microprocessor extension or coprocessor. The address bus is now 24 bits wide to accommodate the 16M bytes of physical memory. The pin-outs of the 8086 and 80286 are illustrated in Figure 2 for comparative purposes. Note that the 80286 does not contain a multiplexed address/data bus.

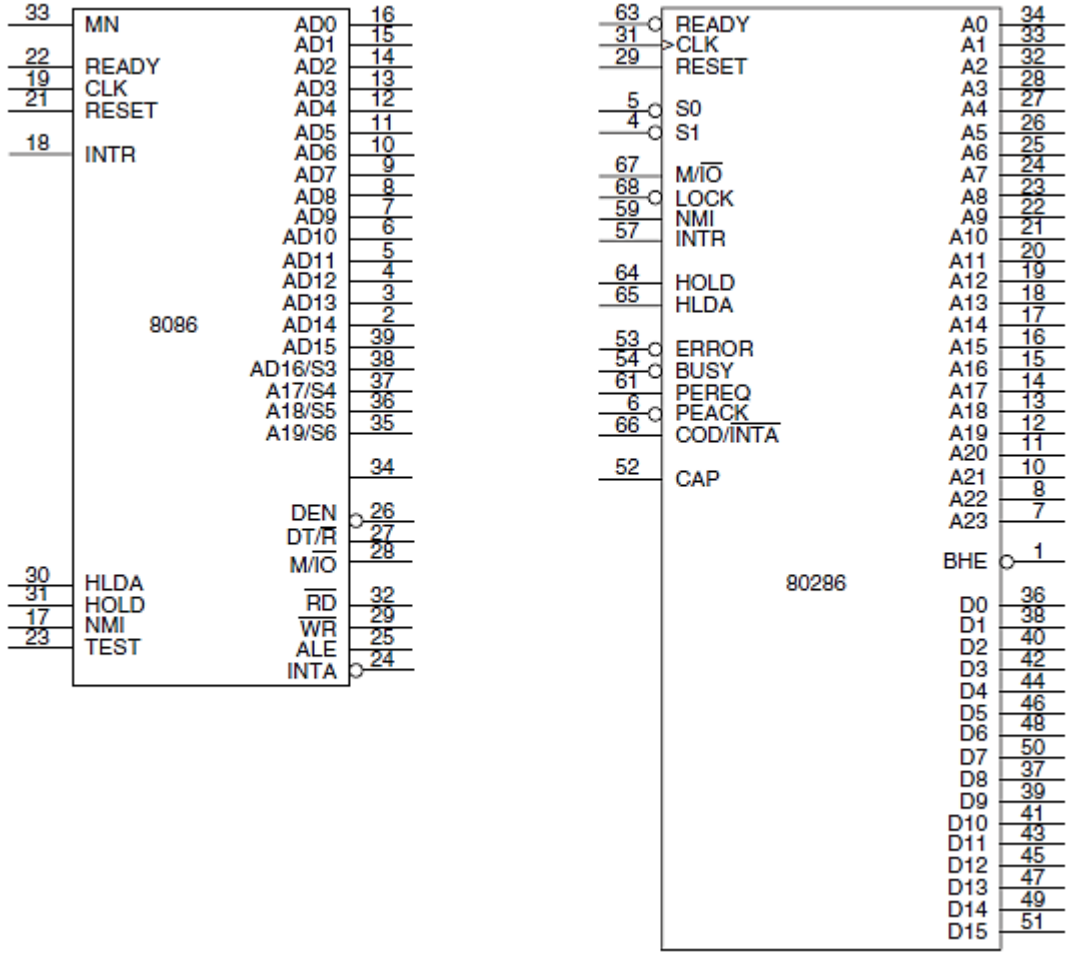

Figure 2. The 8086 and 80286 microprocessor pin-outs.

Memory Management in the Intel 80286

1. **Memory Addressing in 80286**

The 80286 has a 24-bit address bus, allowing it to access 16 MB of physical memory. It supports two memory modes :
Real Mode → Uses 20-bit addressing, limiting it to 1 MB of memory.
Protected Mode → Uses 24-bit addressing, allowing access to 16 MB of memory.

2. **Real Mode Memory Management**

In real mode, the 80286 behaves like an 8086:

Uses segment: offset addressing, meaning memory is accessed in 64 KB segments.
The maximum accessible memory is 1 MB (2^{20} = 1,048,576 bytes).
No memory protection—programs can overwrite each other's memory, leading to instability.
No support for multitasking or virtual memory.

- What is virtual memory.

Virtual memory is that part of hard disk which can be utilized for storing large instructions inside the system. This extra memory can be addressed by the computer other than the physical memory.

3. Protected Mode Memory Management

- Protected mode is where the 80286 truly enhances memory management:
- Support multitasking and virtual memory.

A. Addressing in Protected Mode

-Uses a 24-bit address bus, expanding memory access from 1 MB to 16 MB.
-Introduces logical to physical address translation using segmentation.

B. Segmentation in 80286

- Instead of the simple segmentation model in real mode, protected mode introduces an advanced segmentation system with descriptors.
- Each segment has a Segment Descriptor stored in a Descriptor Table. These descriptors define:
- **Base Address** (Starting location in memory)
- **Limit** (Size of the segment)
- **Access Rights** (Who can access it)

- Types of Descriptor Tables

1- Global Descriptor Table (GDT) → Stores global segments used by all programs.
2- Local Descriptor Table (LDT) → Stores segments specific to a particular process.
3- Interrupt Descriptor Table (IDT) → Stores interrupt service routines.

Additional Instructions

- The 80286 has even more instructions than its predecessors. These extra instructions control the virtual memory system through the memory manager of the 80286.
- Table 1 lists the additional 80286 instructions with a comment about the purpose of each instruction.

Table 1. Additional 80286 instructions.

Instruction	*Purpose*
CLTS	Clear the task-switched bit
LDGT	Load global descriptor table register
SGDT	Store global descriptor table register
LIDT	Load interrupt descriptor table register
SIDT	Store interrupt descriptor table register
LLDT	Load local descriptor table register
SLDT	Store local descriptor table register
LMSW	Load machine status register
SMSW	Store machine status register
LAR	Load access rights
LSL	Load segment limit
SAR	Store access rights
ARPL	Adjust requested privilege level
VERR	Verify a read access
VERW	Verify a write access

Register Organization in Intel 80286

- The Intel 80286 has a 16-bit register architecture, similar to the 8086, but with enhancements for protected mode. The registers are divided into the following categories:

1. General-Purpose Registers (GPRs)

These 16-bit registers are used for data operations, calculations, and memory access (AX, BX,CX,DX)

2. Segment Registers (16-bit)

The 80286 uses segmentation, and these registers hold the base addresses of memory segments. Which are (CS, SS, DS, ES)

3. Pointer and Index Registers

These are used for memory addressing and stack operations. Which are (SP, BP, SI, DI)

4. Instruction Pointer (IP)

-In real mode, IP is used with CS (CS:IP) to determine the next instruction.
-In protected mode, it works with segmentation and descriptors.

5. Status and Control Registers

A. Flags Register (16-bit)

(CF, PF, ZF, SF, TF, IF, DF, OF)

B. Machine Status Word (MSW)

-Used only in protected mode.
-Controls CPU operating mode (real/protected mode).
-CR0 Register (part of MSW) is introduced for mode switching.

- **PE (bit D16**) Protection enable flag places the 80286 in protected mode, when PE is set. This can only he cleared by resetting the CPU.
- PE=0 >>>In real mode
- PE=1>>>In protected mode

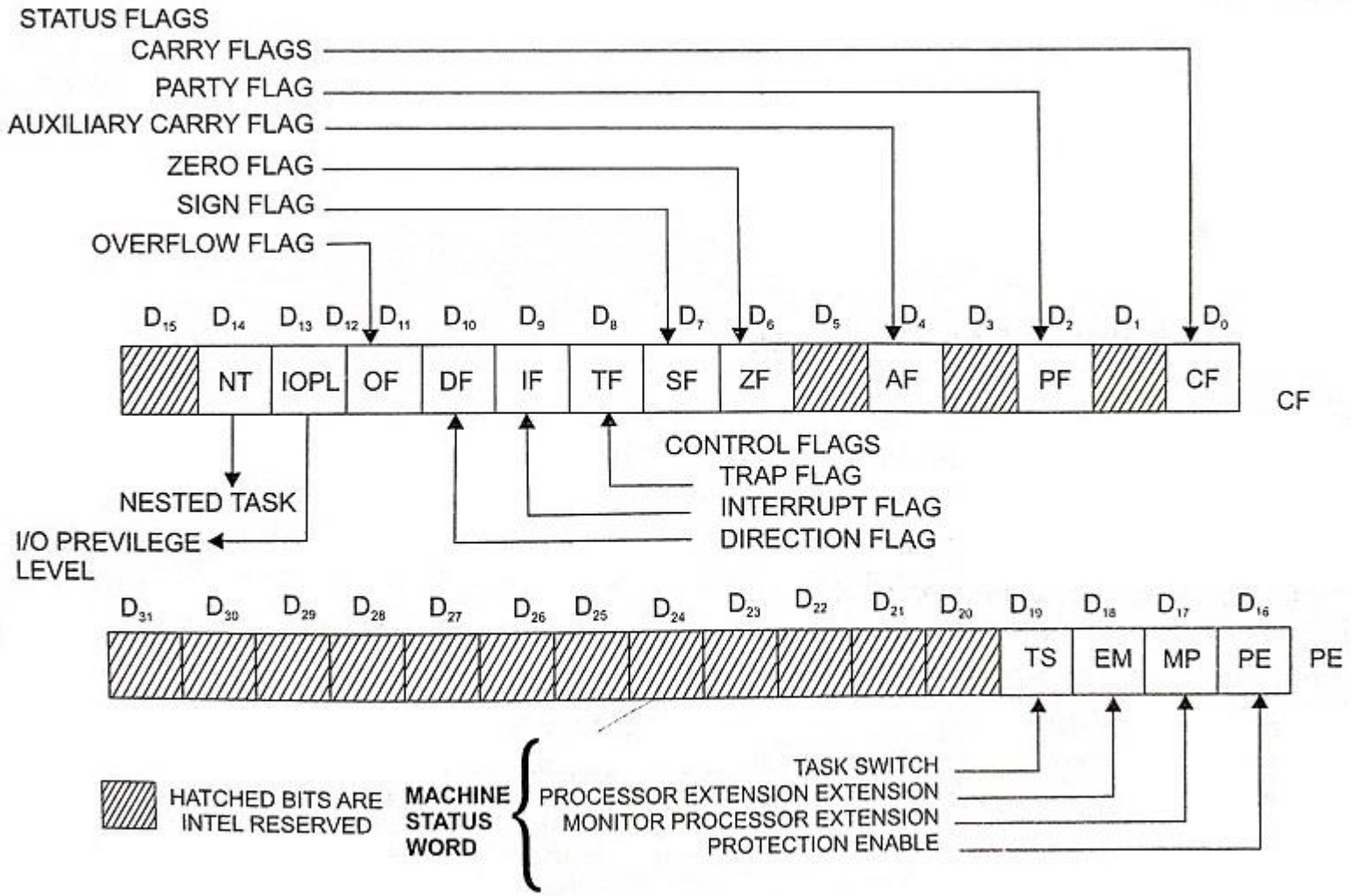

Fig. 3 *80286 flag registers*

- **MP (bit D17)** When MP is set. the monitor processor extension flag allows WAIT instruction to generate a processor extension not present in the exception.
- **EM (bit D18)** If EM is set, the emulate processor extension nag causes a processor extension absent exception and permits the emulation of processor extension by CPU.
- **TS (bit D19)** When TS set, this flag indicates the next instruction using extension will generate exception 7, permitting the CPU to test whether the current processor extension is for the current task.

البت	الاسم	الوظيفة
MP	Monitor Processor	يُستخدم للتحكم في عمليات المعالجة المتعددة (Multiprocessing). عند تعيينه، يمكن أن يشير إلى أن المعالج يعمل في بيئة متعددة المعالجات، ويؤثر على سلوك تعليمة `WAIT`.
EM	Emulation	يُستخدم للإشارة إلى محاكاة المعالج الرياضي المشترك (FPU). إذا تم تعيينه، فإن التعليمات الخاصة بوحدة الفاصلة العائمة (مثل `ESC` الخاصة بـ 8087) يتم تنفيذها عبر المحاكاة البرمجية بدلاً من المعالج الرياضي المخصص.
TS	Task Switched	يتم تعيينه تلقائيًا عند التبديل بين المهام (Tasks) في وضع الحماية (Protected Mode). يُستخدم من قبل نظام التشغيل لتحديد ما إذا كان يجب حفظ أو استعادة سياق المعالج المشترك الرياضي عند التبديل بين العمليات.

البت	الاسم	القيمة = 0	القيمة = 1
MP	Monitor Processor	تعليمة `WAIT` تعمل بدون فحص `TS`.	تعليمة `WAIT` تتحقق من `TS` قبل تنفيذ أي تعليمات خاصة بالمعالج الرياضي المشترك (FPU).
EM	Emulation	المعالج يدعم وحدة الفاصلة العائمة (FPU) مثل 8087.	يتم محاكاة تعليمات الفاصلة العائمة برمجيًا بدلاً من استخدام المعالج الرياضي المشترك.
TS	Task Switched	لم يتم تبديل المهمة، وبالتالي لا يلزم حفظ أو استعادة حالة المعالج المشترك.	تم تبديل المهمة، مما يشير إلى ضرورة حفظ أو استعادة حالة المعالج المشترك الرياضي عند استخدام `WAIT` أو تعليمات الفاصلة العائمة.

6. Task Register (TR)

-Used in protected mode to store information about the current task.
-Points to the Task State Segment (TSS), which stores task-specific data.

- **IOPL (I/O Privilege Level)** [Bits 12-13] – Defines privilege levels for I/O operations.

- **NT (Nested Task) [Bit 14] –** Used for task switching.

يتم استخدامه في **وضع الحماية (Protected Mode)** عند تنفيذ مهام متداخلة
عندما يكون NT=1 فان ايعاز IRET يعالج المهمة على اتها متداخلة مما يعني استعادة المهمة السابقة بدلا من انهائها بالكامل
عندما يكون NT=0 فان ايعاز IRET يقوم بانهاء المهمة بدلا من العودة الى المهمة السابقة كمتداخلة

7. Descriptor Table Registers (Protected Mode Only)

These registers are used in protected mode to store segment descriptors.

Register	Purpose
GDTR (Global Descriptor Table Register)	Holds the address of the Global Descriptor Table (GDT).
LDTR (Local Descriptor Table Register)	Holds the address of the Local Descriptor Table (LDT).
IDTR (Interrupt Descriptor Table Register)	Holds the address of the Interrupt Descriptor Table (IDT).

Privilege Levels: مستوى الصلاحية

- The 80286 supports four privilege levels (0 to 3), with 0 being the most privileged (kernel mode وضع النواة) and 3 being the least privileged (user mode وضع المستخدم).
- Privilege levels are used to restrict access to critical system resources and ensure that user programs cannot interfere with the operating system or other tasks.

- Protection Mechanism in 80286
  Based on:
  Memory segmentation
  Privilege levels

- Level 0 (Highest Privilege):
  Reserved for the operating system kernel and critical system software.
  Has unrestricted access to all system resources, including memory and hardware.
- Level 1 and Level 2:
  Typically used for system services or device drivers.
  Have limited access to resources, depending on the operating system's design.
- Level 3 (Lowest Privilege):
  Used for user applications.
  Has the most restricted access to system resources to prevent accidental or malicious interference with the system.

مثال عملي:

عند تشغيل تطبيق مثل متصفح الإنترنت على جهازك، يعمل هذا التطبيق في **مستوى امتياز 3** (وضع المستخدم). إذا حاول التطبيق الوصول إلى جزء من الذاكرة محجوز للنواة (مستوى 0)، فإن المعالج يمنع هذا الوصول للحفاظ على أمان النظام.